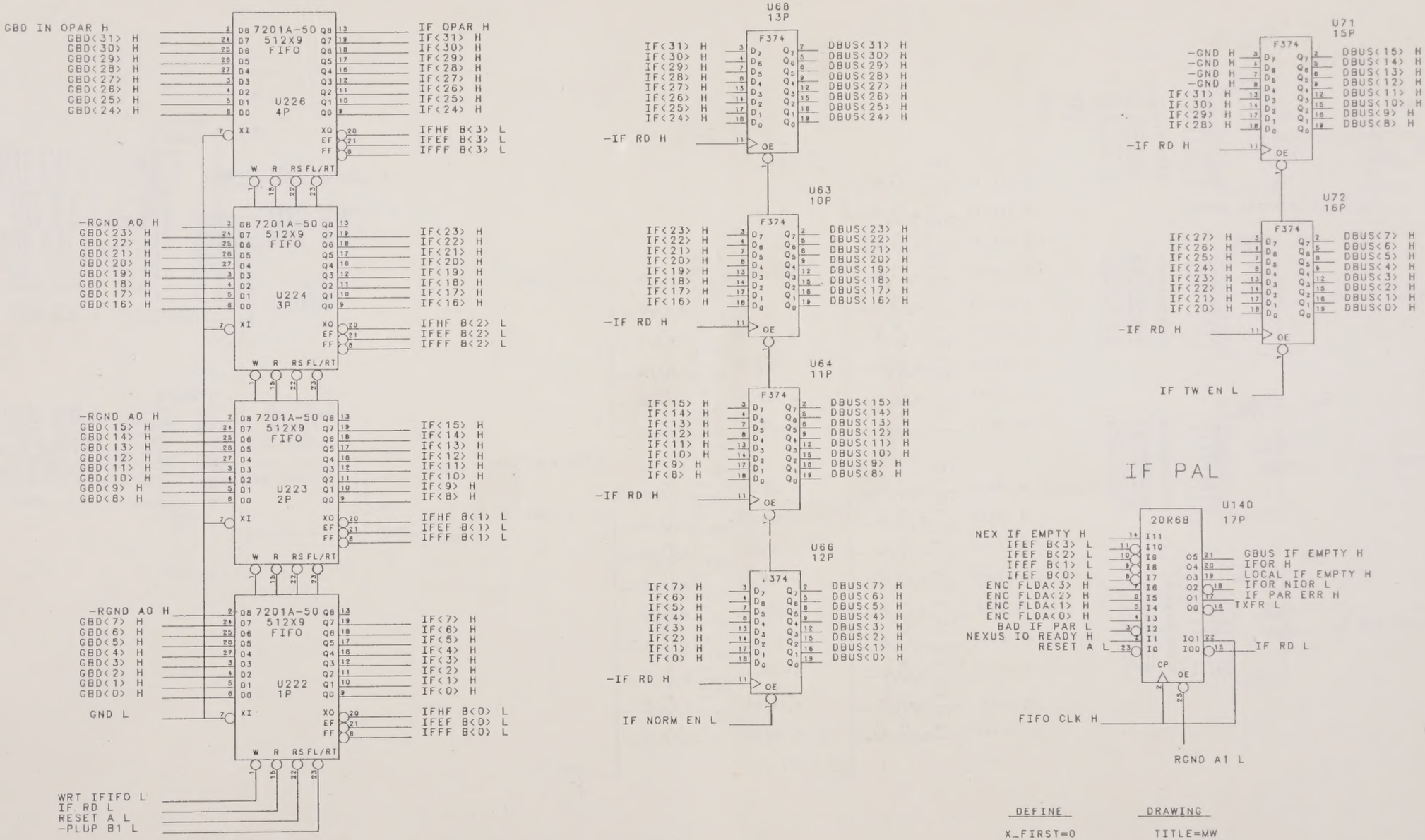

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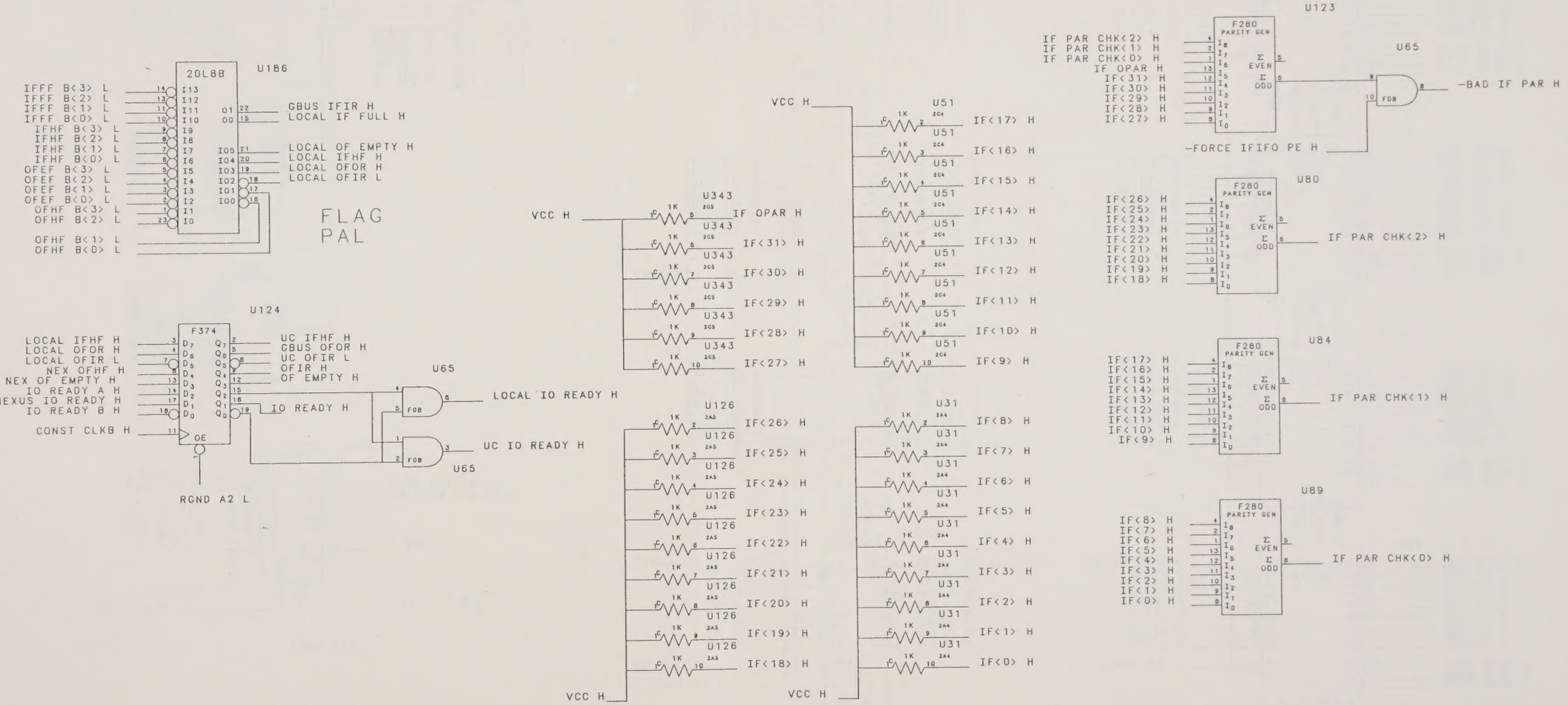
ENGINEER:	DRAWN BY: t.moser	PAGE: 1



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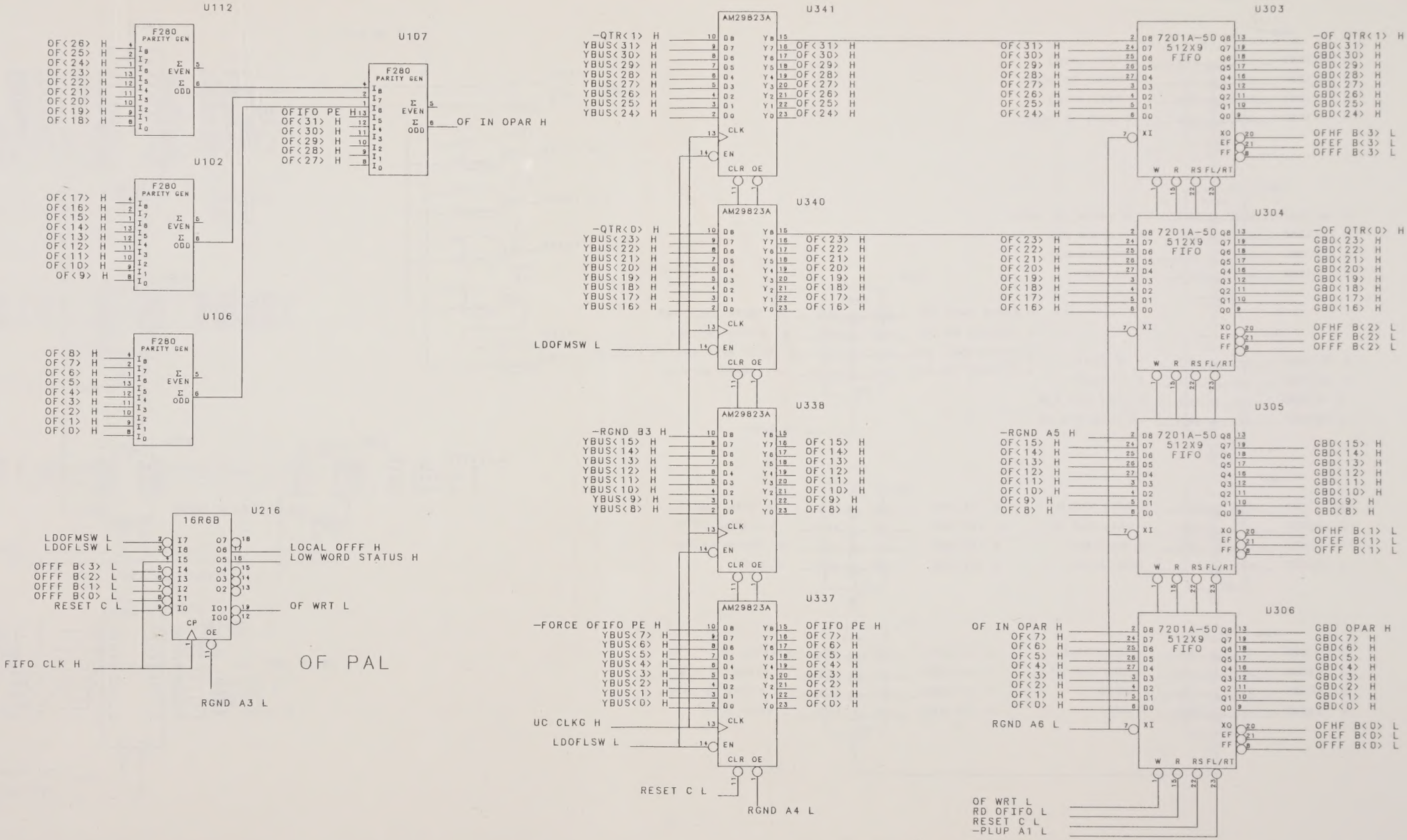

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TITLE:		DATE:
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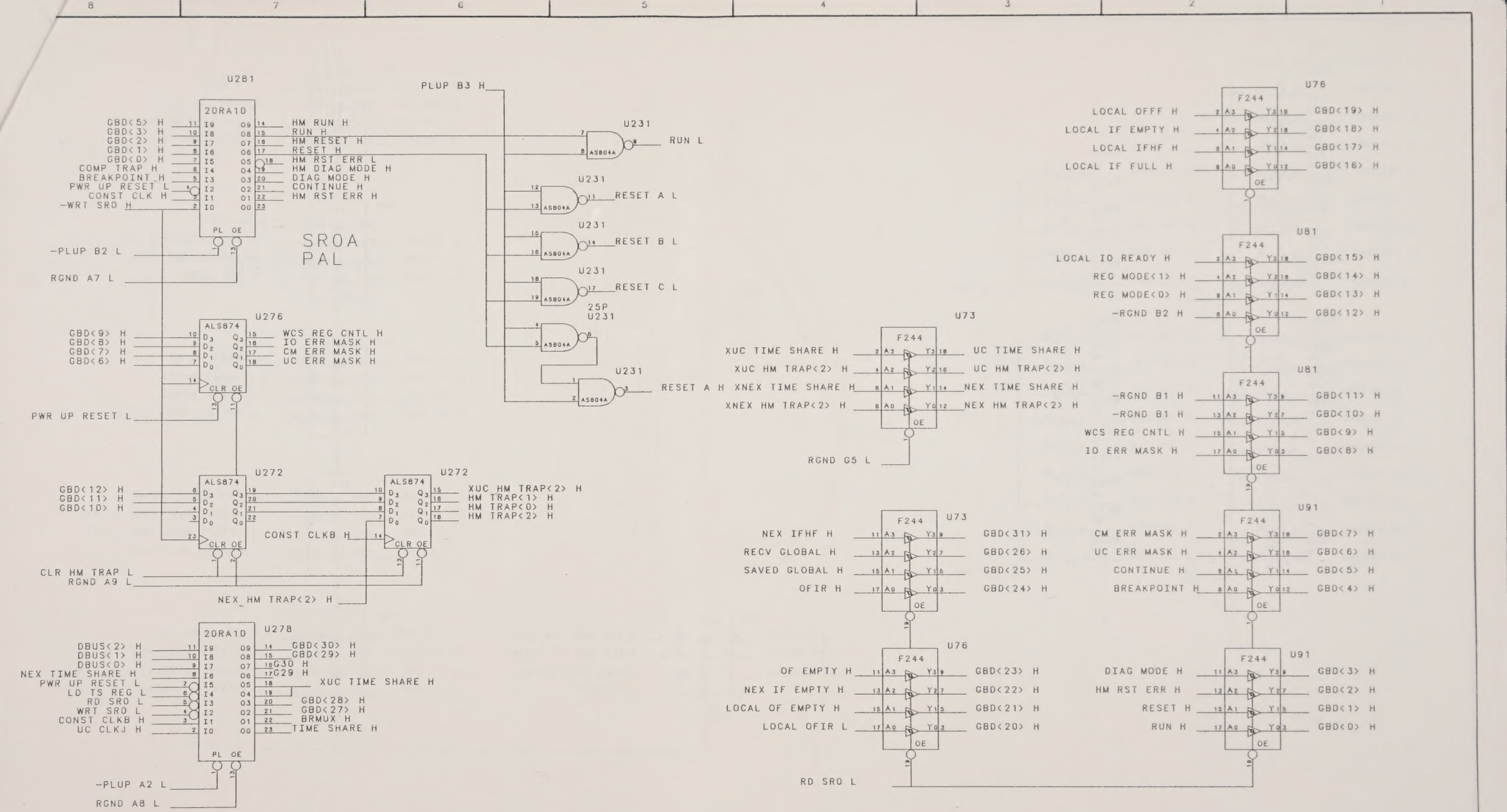
ENGINEER:	DRAWN BY: t.moser	PAGE: 3



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TITLE:		DATE:
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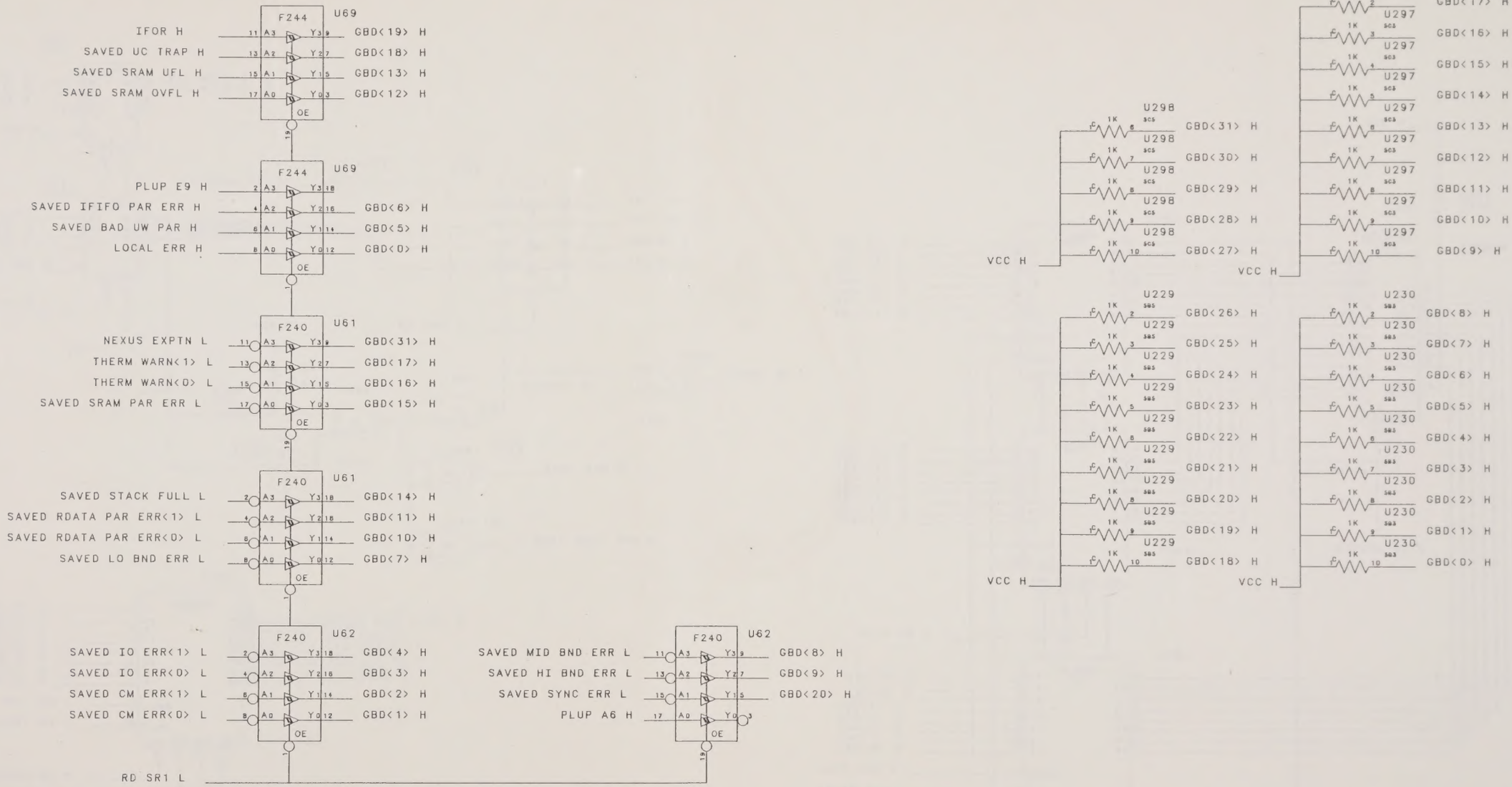
ENGINEER: JIM LALONE	DRAWN BY:	PAGE: 4



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TITLE: READ REGISTER 1 REV 4	DATE: 7/7/87
ENGINEER: JIM LALONE	DRAWN BY:
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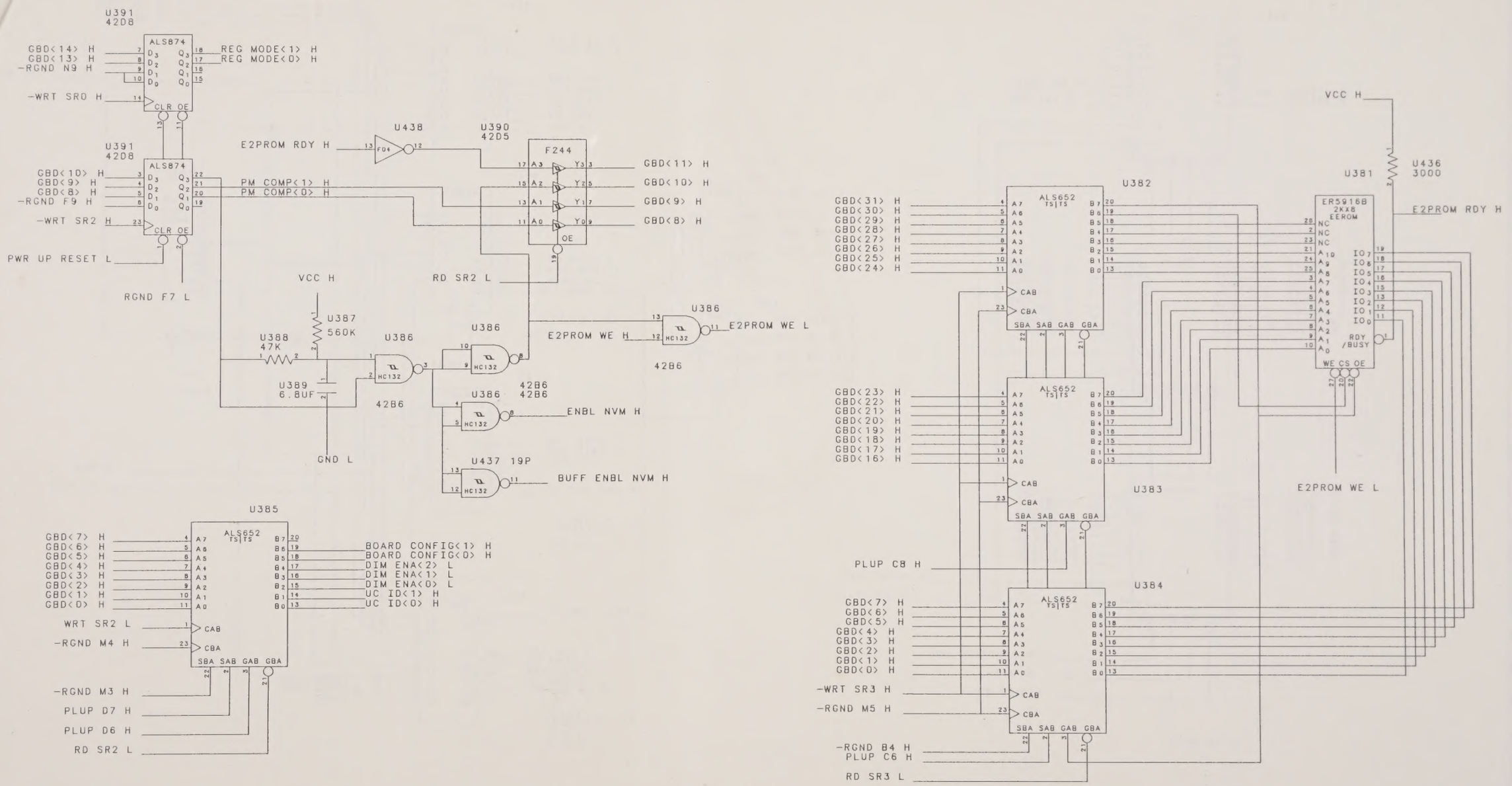

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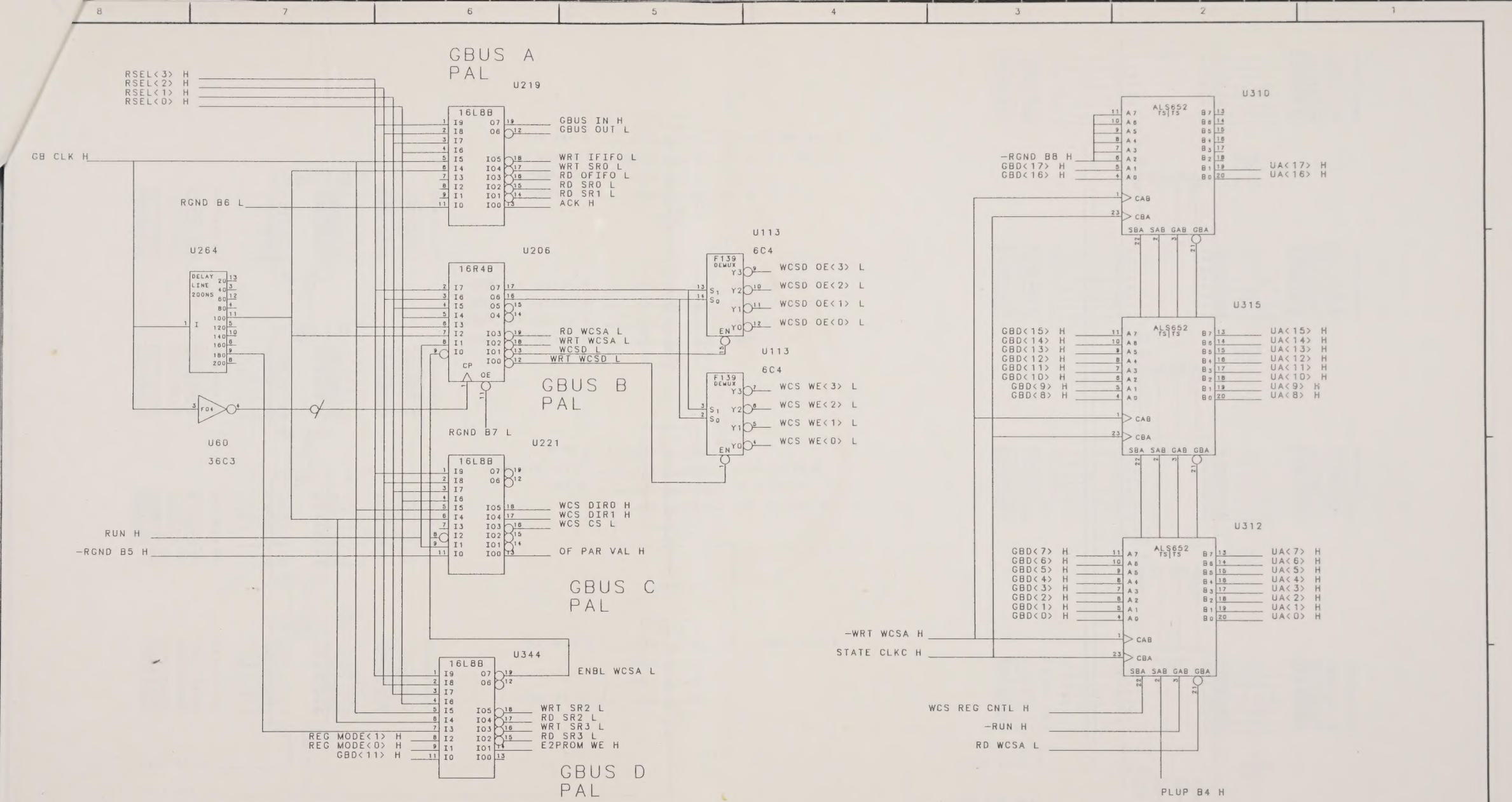
TITLE:	DATE:
STATUS REGISTER 2,3 AND NON-VOLITLE RAM	7/11/87
ENGINEER: JIM LALONE / DRAWN BY:	PAGE: 6



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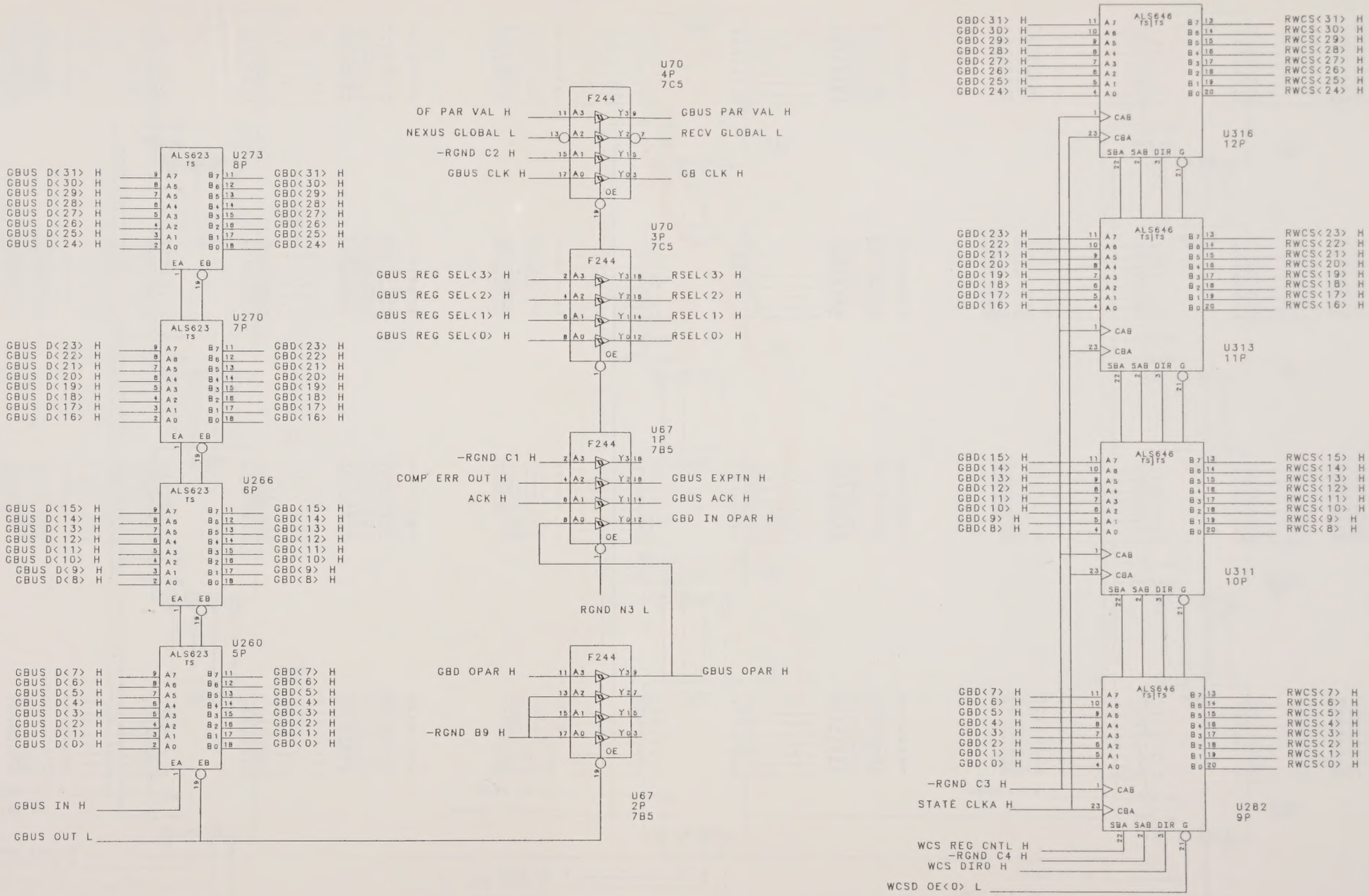
TITLE: GBUS REGISTER DECODE REV 4		DATE: 7/11/87
ENGINEER: JIM LALONE	DRAWN BY:	PAGE: 7



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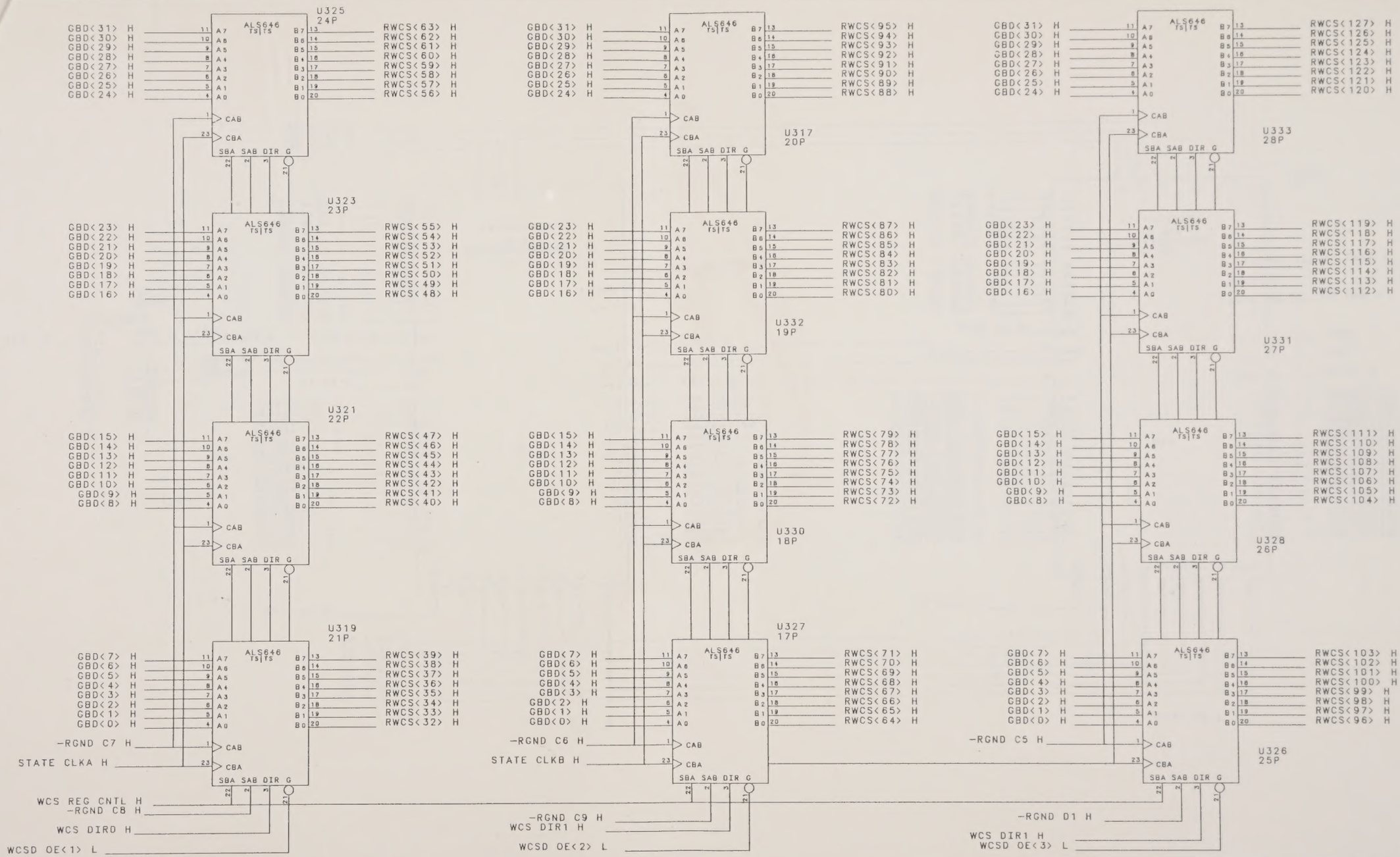
TITLE: GBUS TRANSIEVERS REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser

PAGE: 8



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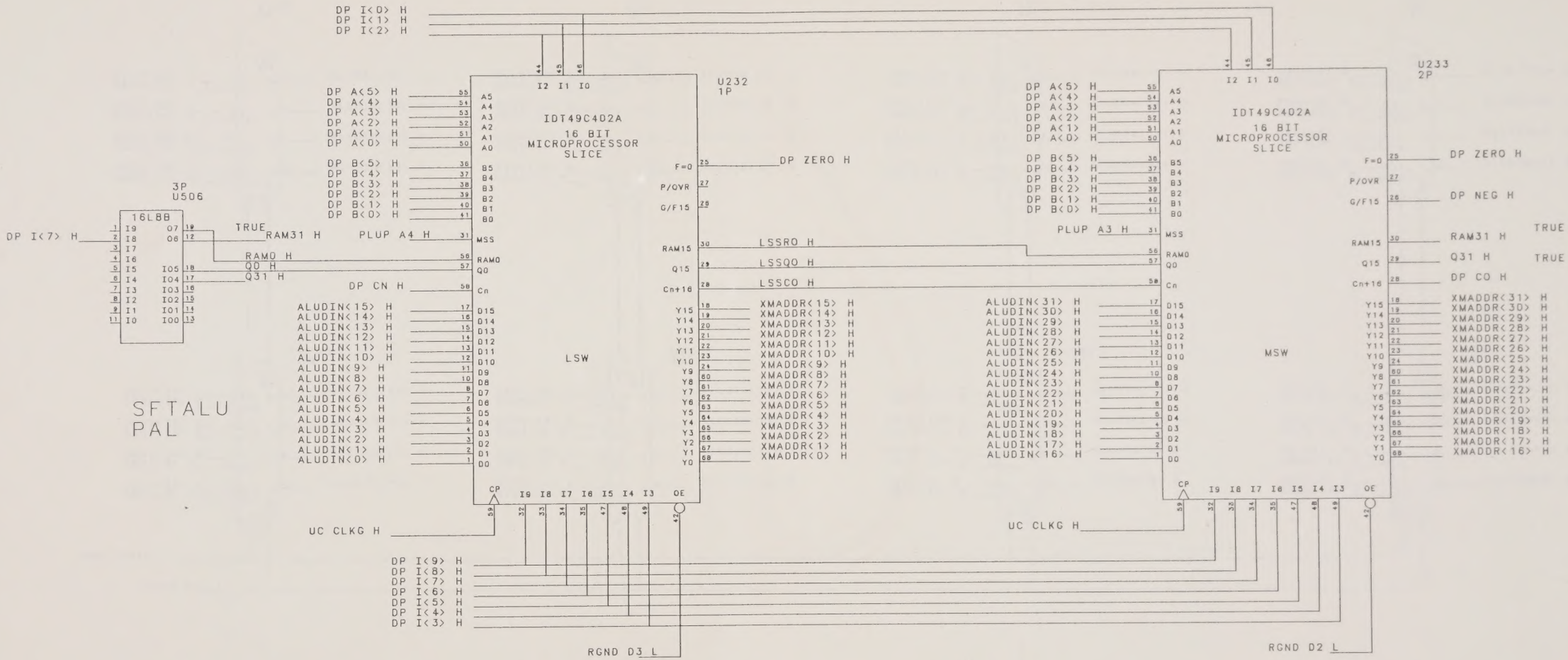
TITLE: CONTROL STORE DOWNLOAD PATH REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser



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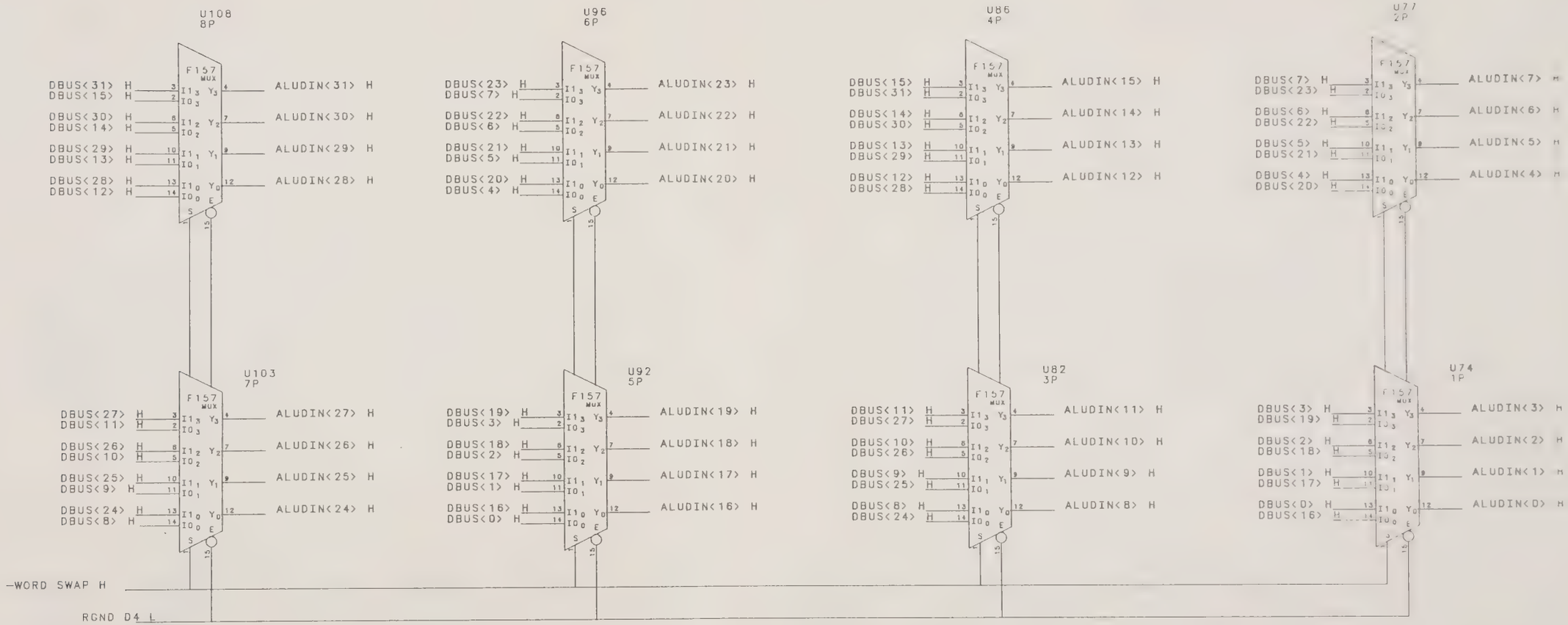
TITLE: ALU'S	REV 4	DATE: 7/11/87
ENGINEER:	DRAWN BY: t.moser	PAGE: 10



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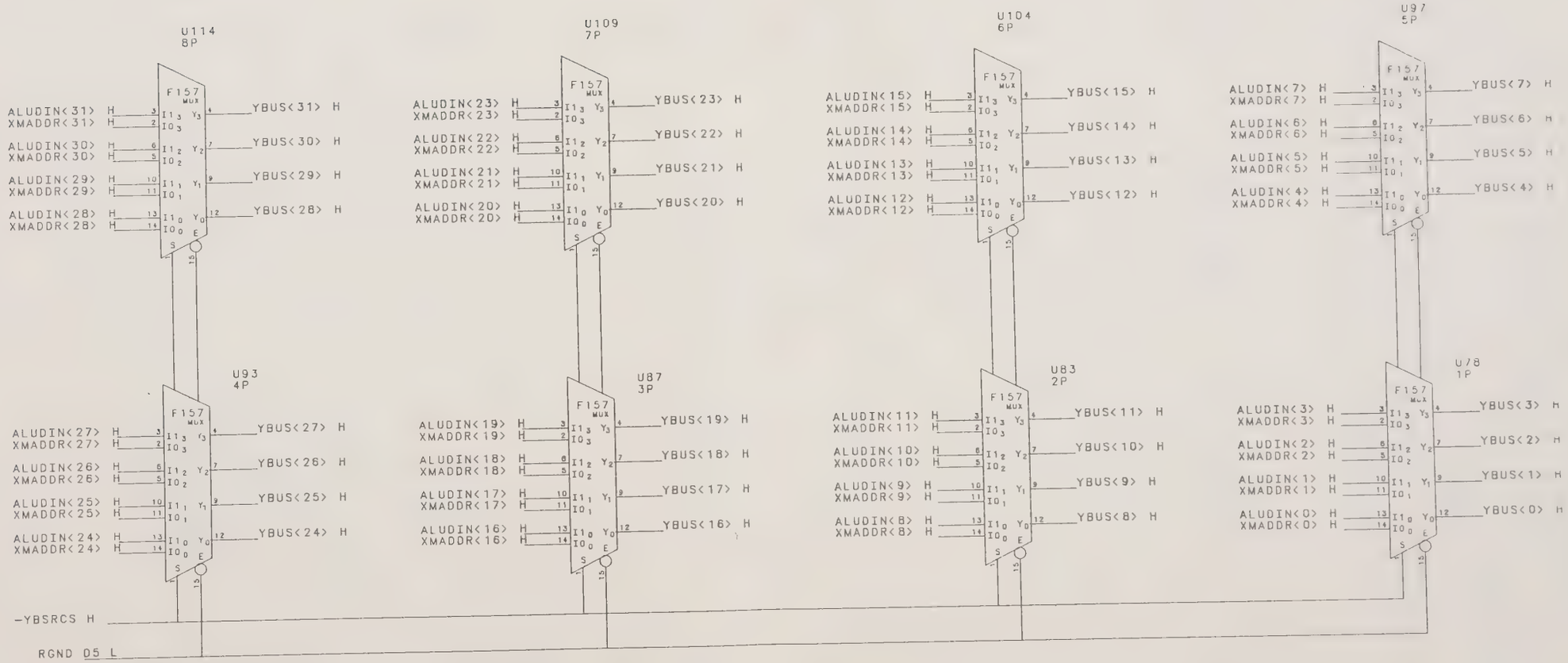
TITLE: WORD SWAPPERS

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser



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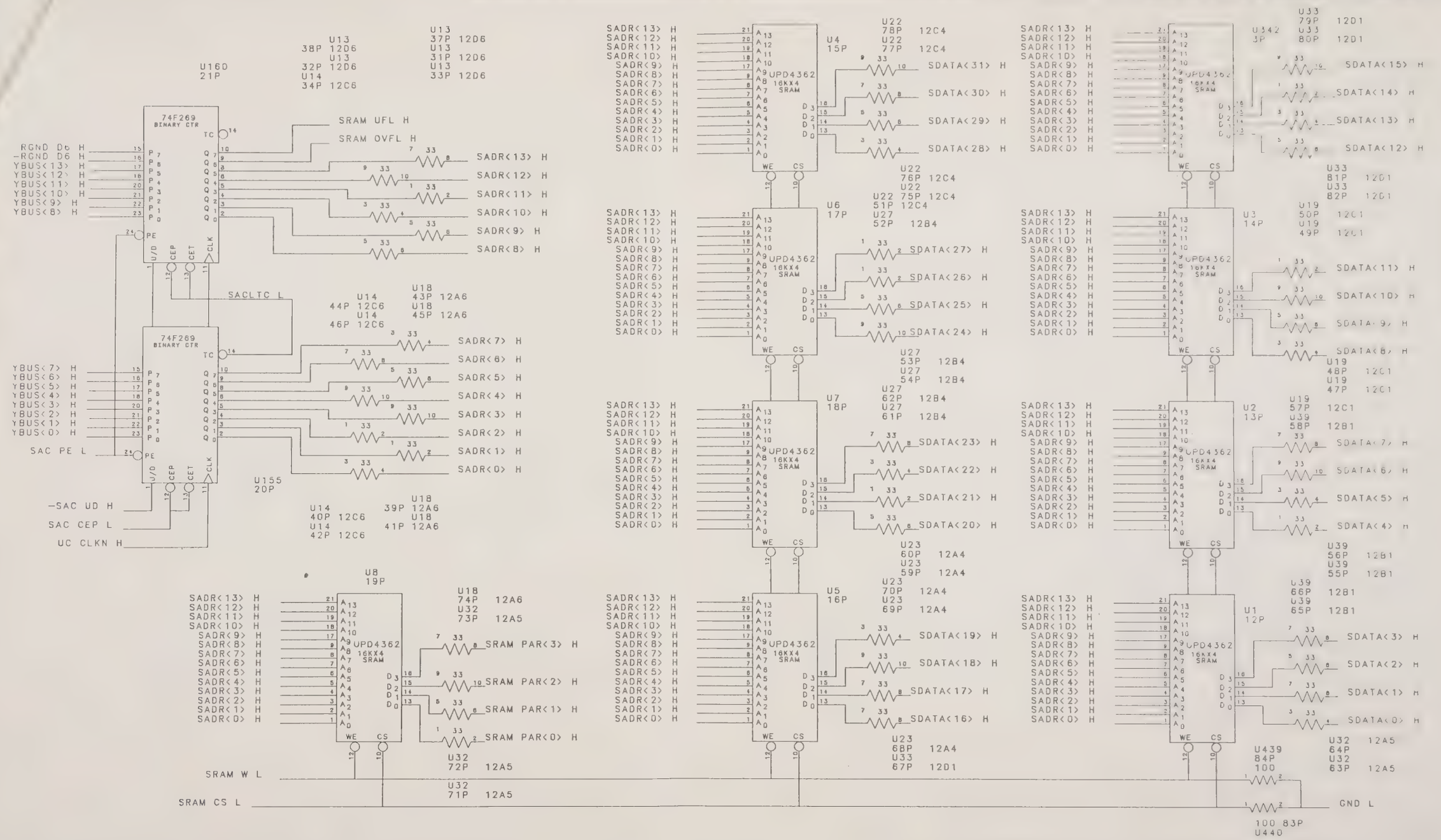
TITLE: YBUS SOURCE SELECT MUX

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser

PAGE: 12



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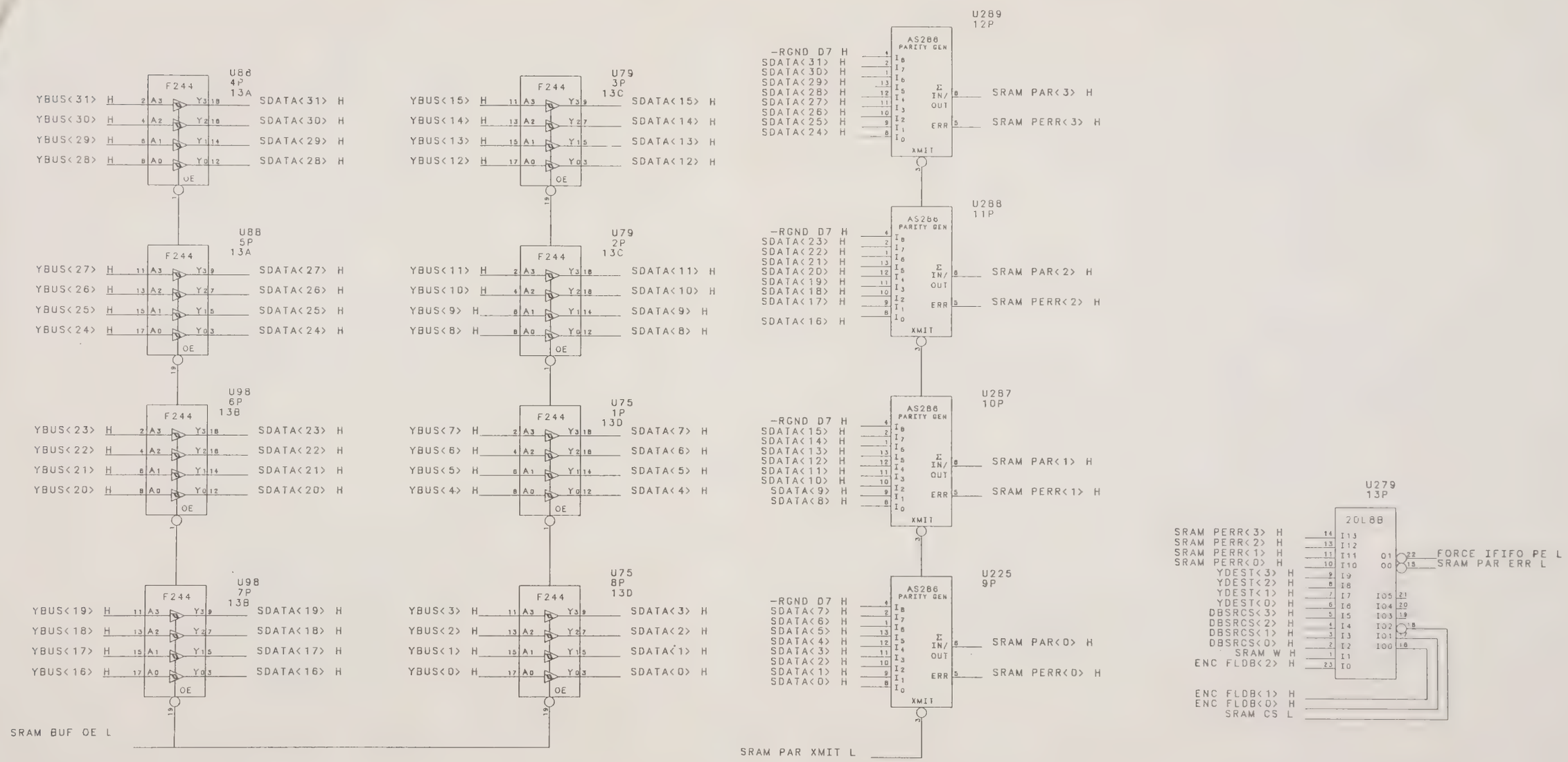
TITLE: SCRATCH MEMORY AND ADDRESS COUNTER

ENGINEER:

DRAWN BY: t.moser

DATE: 7/11/87

PAGE: 13



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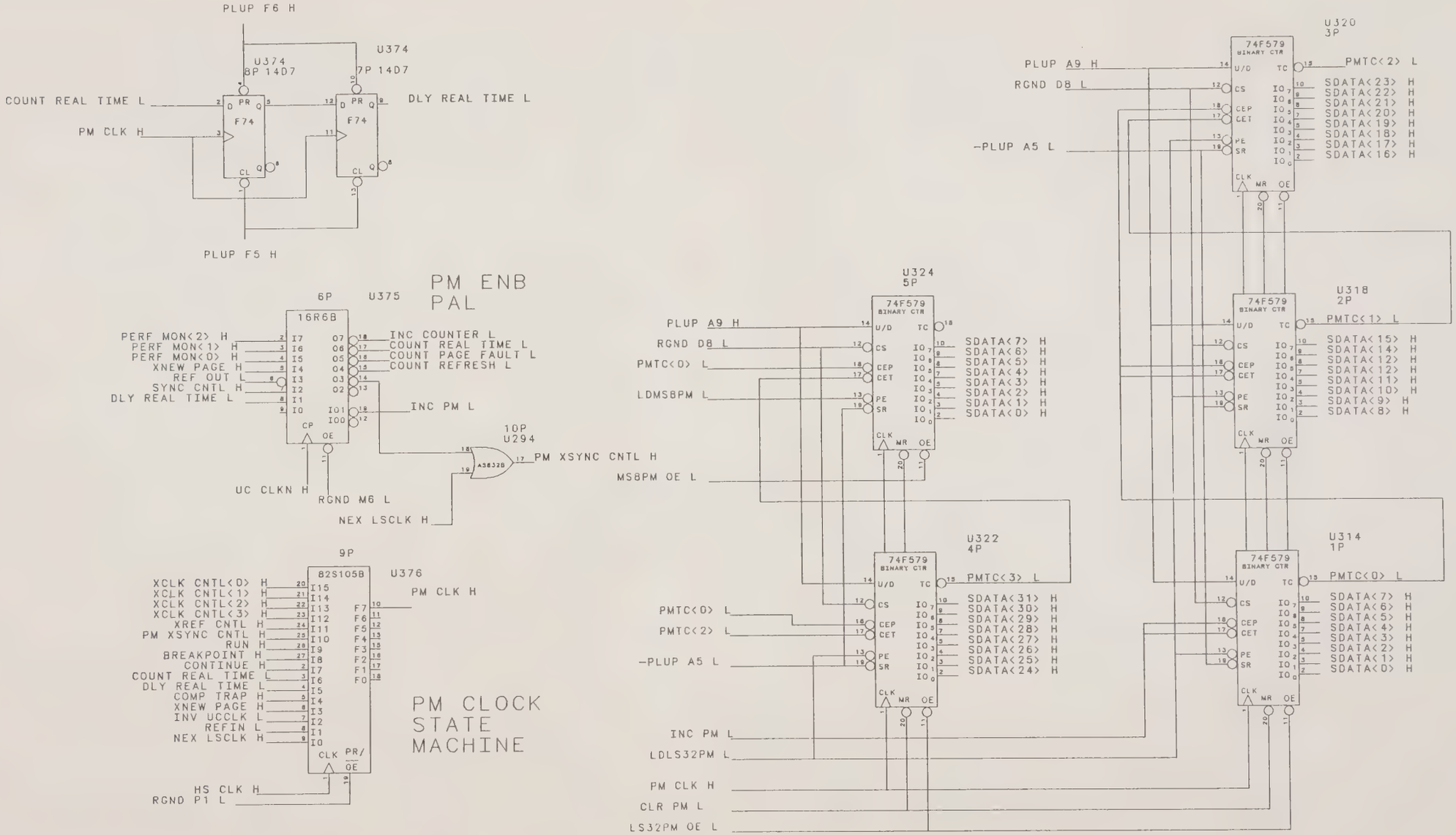
TITLE: YBUS TO SCRATCH RAM BUFFERS AND SCRATCH RAM PARITY GEN/CHK

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser

PAGE: 14



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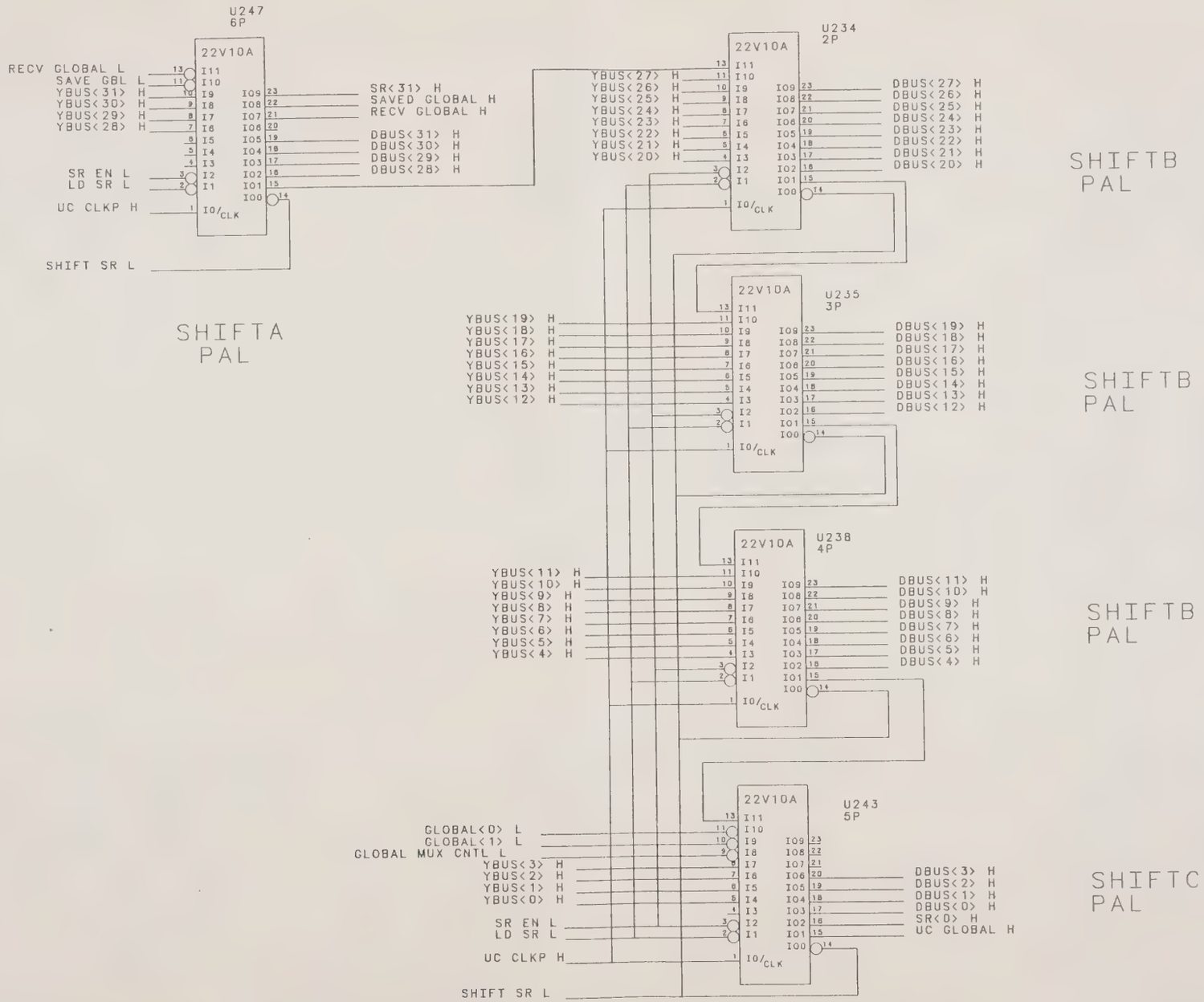
TITLE: PERFORMANCE MONITOR REV 4		DATE: 7/11/87
ENGINEER:	DRAWN BY:	PAGE: 15



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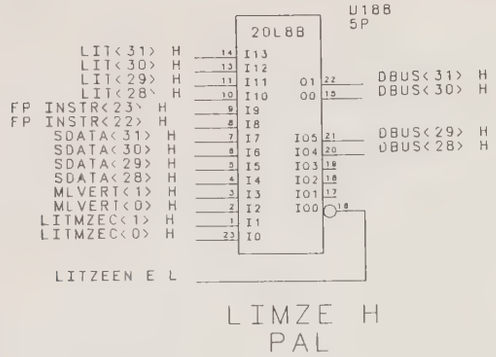
TITLE:	DATE:
GLOBAL SHIFT REGISTER	7/11/87
ENGINEER:	DRAWN BY: t.moser
	PAGE: 16



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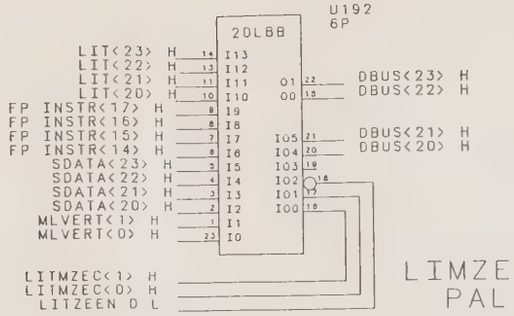

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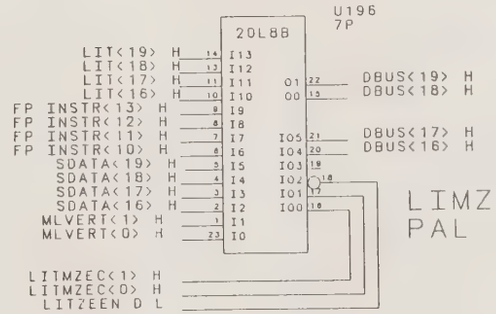

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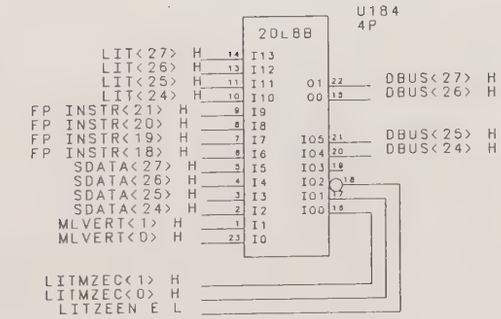

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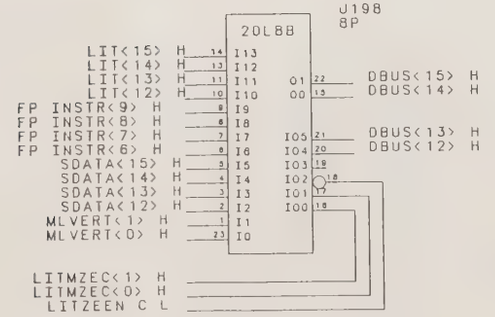

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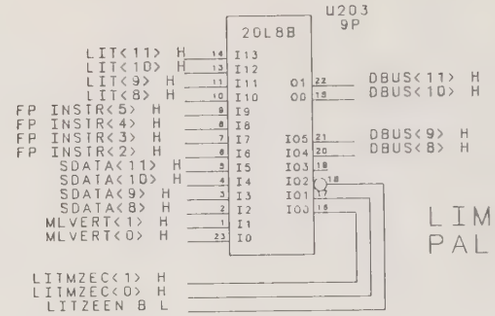

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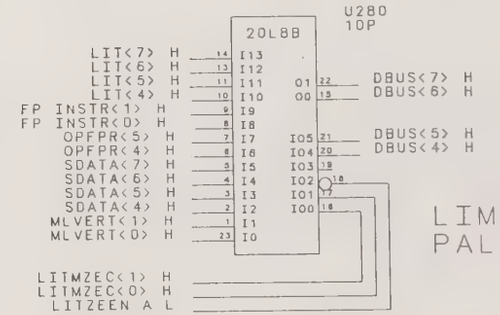

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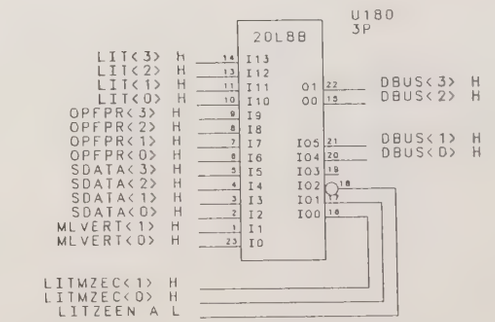

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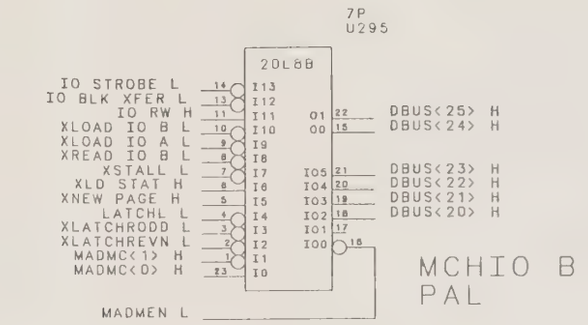
TITLE: LITERAL MUX AND ZERO EXTEND REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY:

PAGE: 17



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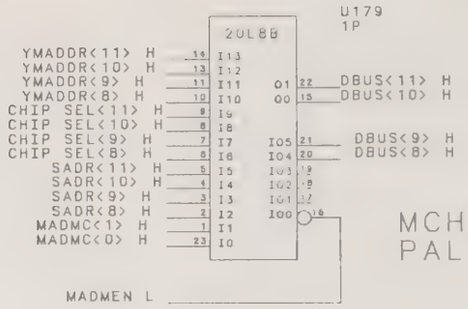

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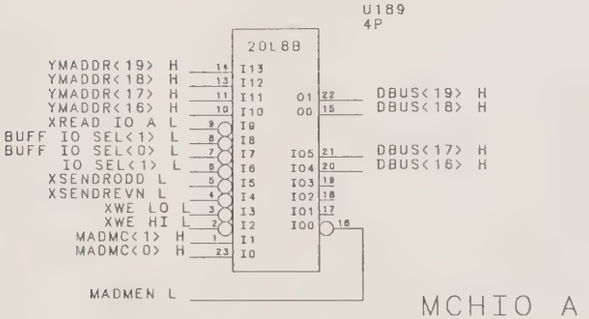

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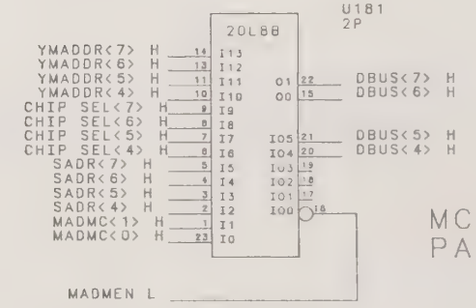

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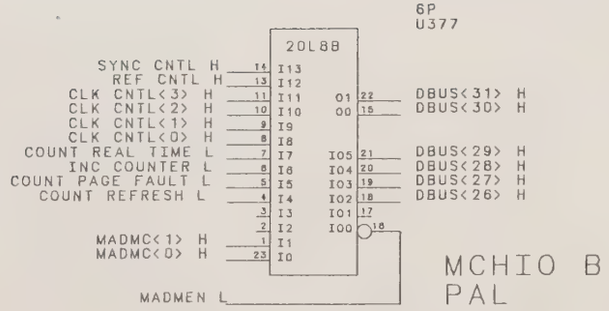

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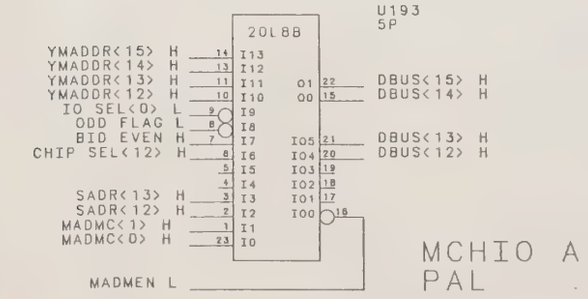

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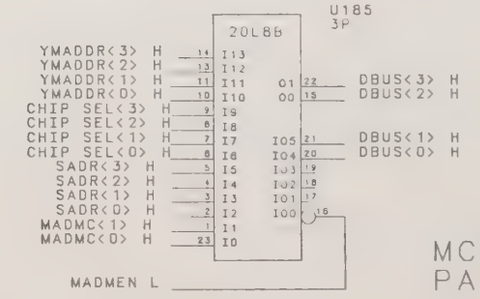

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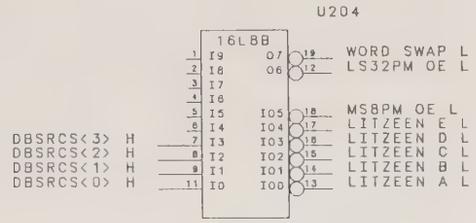
TITLE: MADDR / CHIP-IO SEL / SCRATCH ADDRESS MUX & DBUS SOURCE CONTROL

DATE: 7/11/87

ENGINEER: MAHESH GANMUKI

DRAWN BY: t.moser

PAGE: 18



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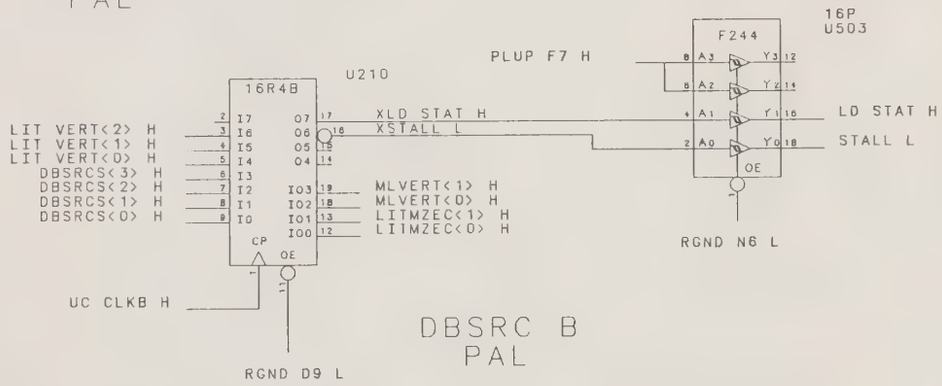

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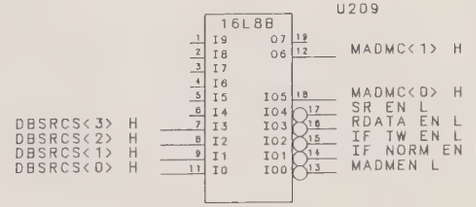

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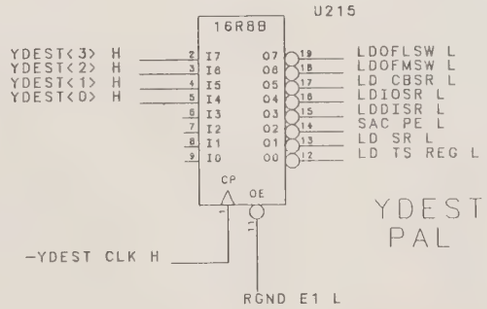

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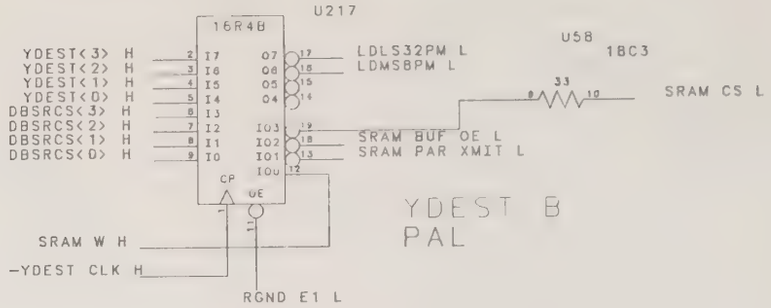

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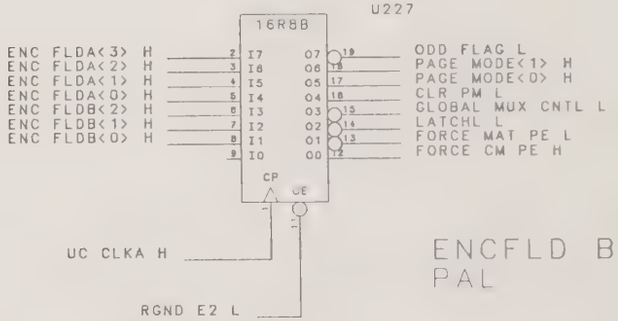

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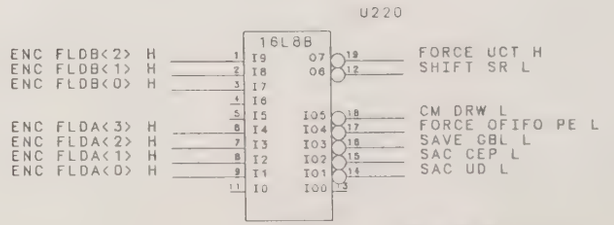

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TITLE: DBUS SOURCE / YBUS DEST CONTROL REV 4

DATE: 7/11/87

ENGINEER:

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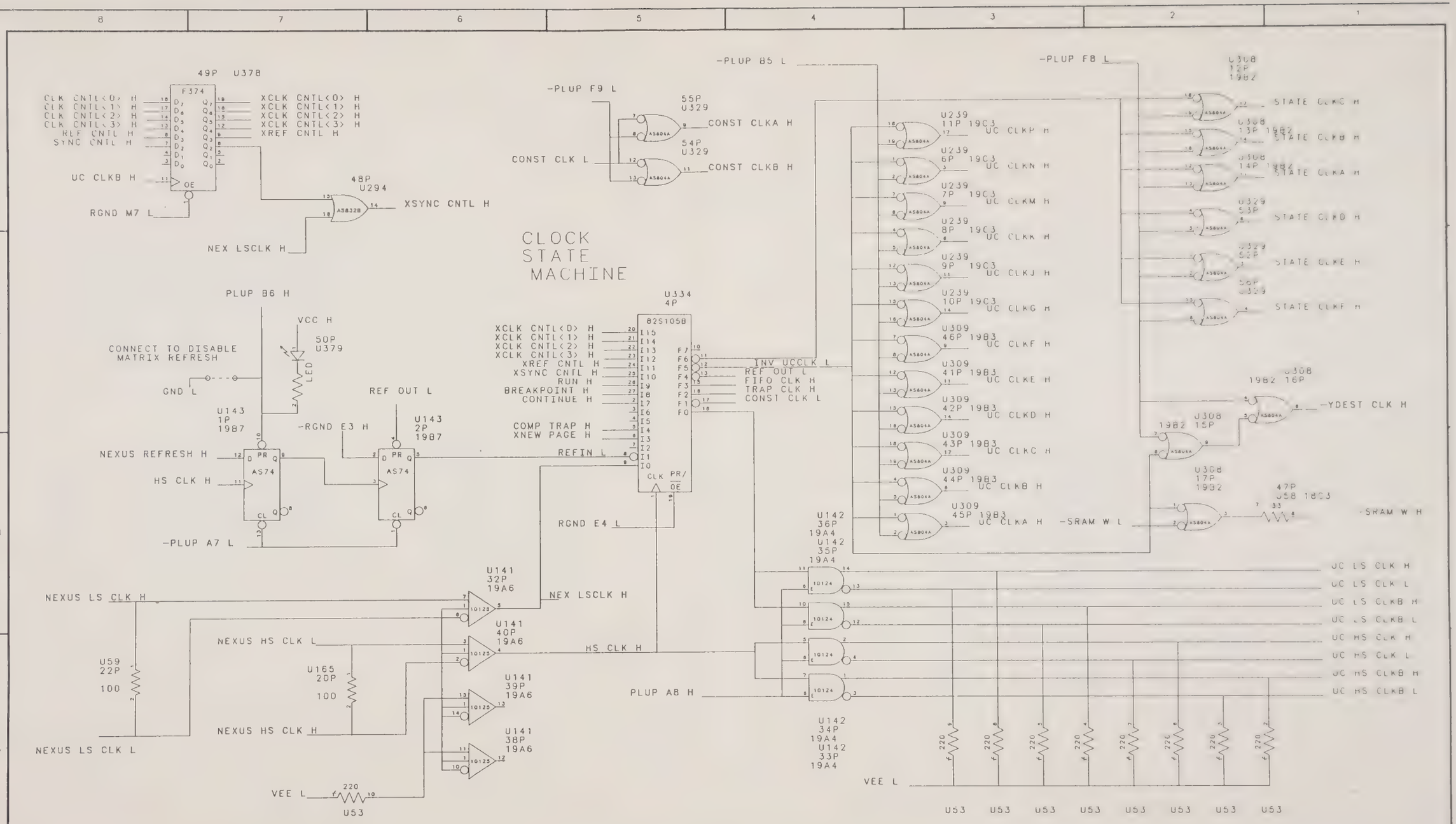

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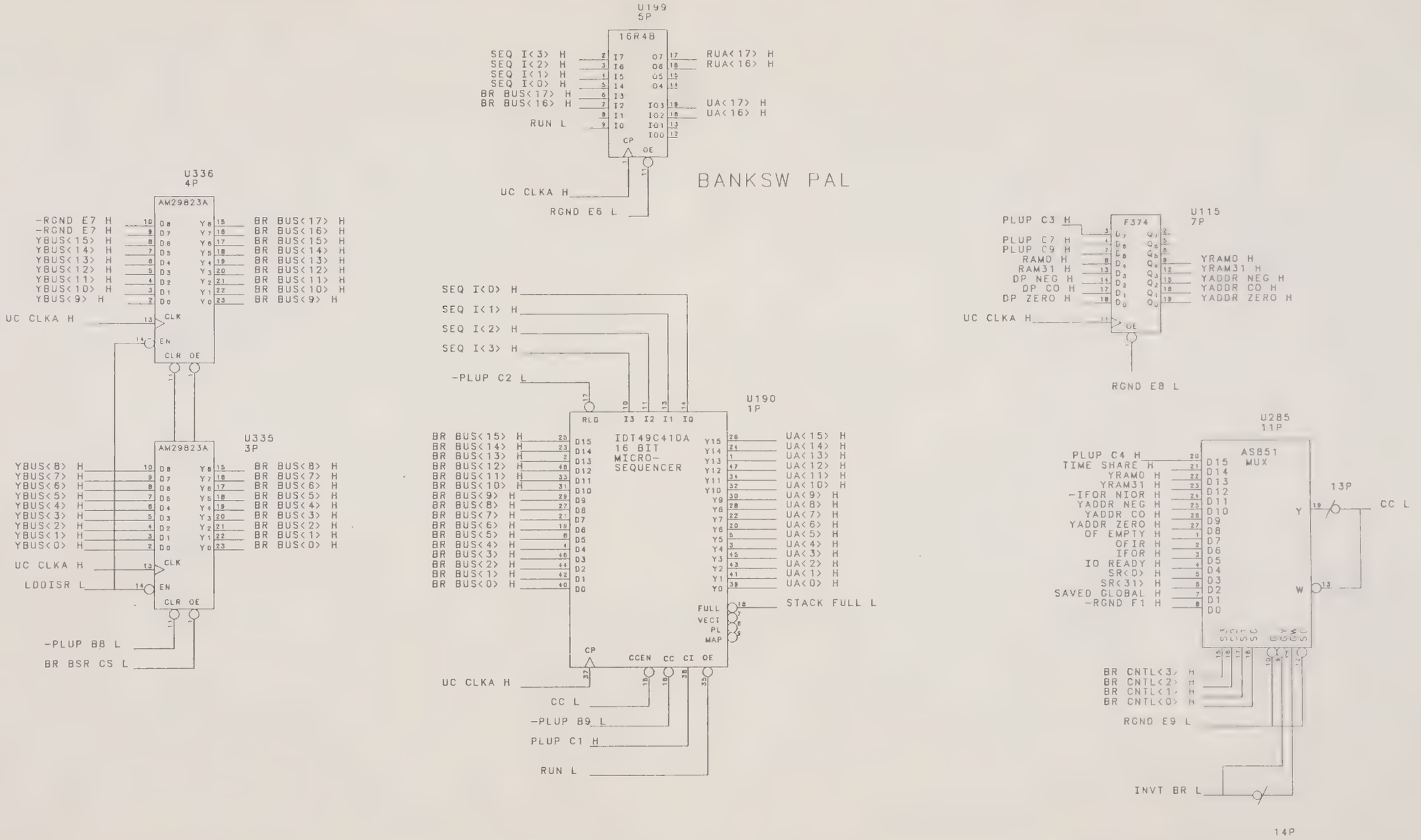
TITLE:		DATE:
CLOCK CIRCUITS	REV 4	7/11/87
ENGINEER:	DRAWN BY:	PAGE: 20



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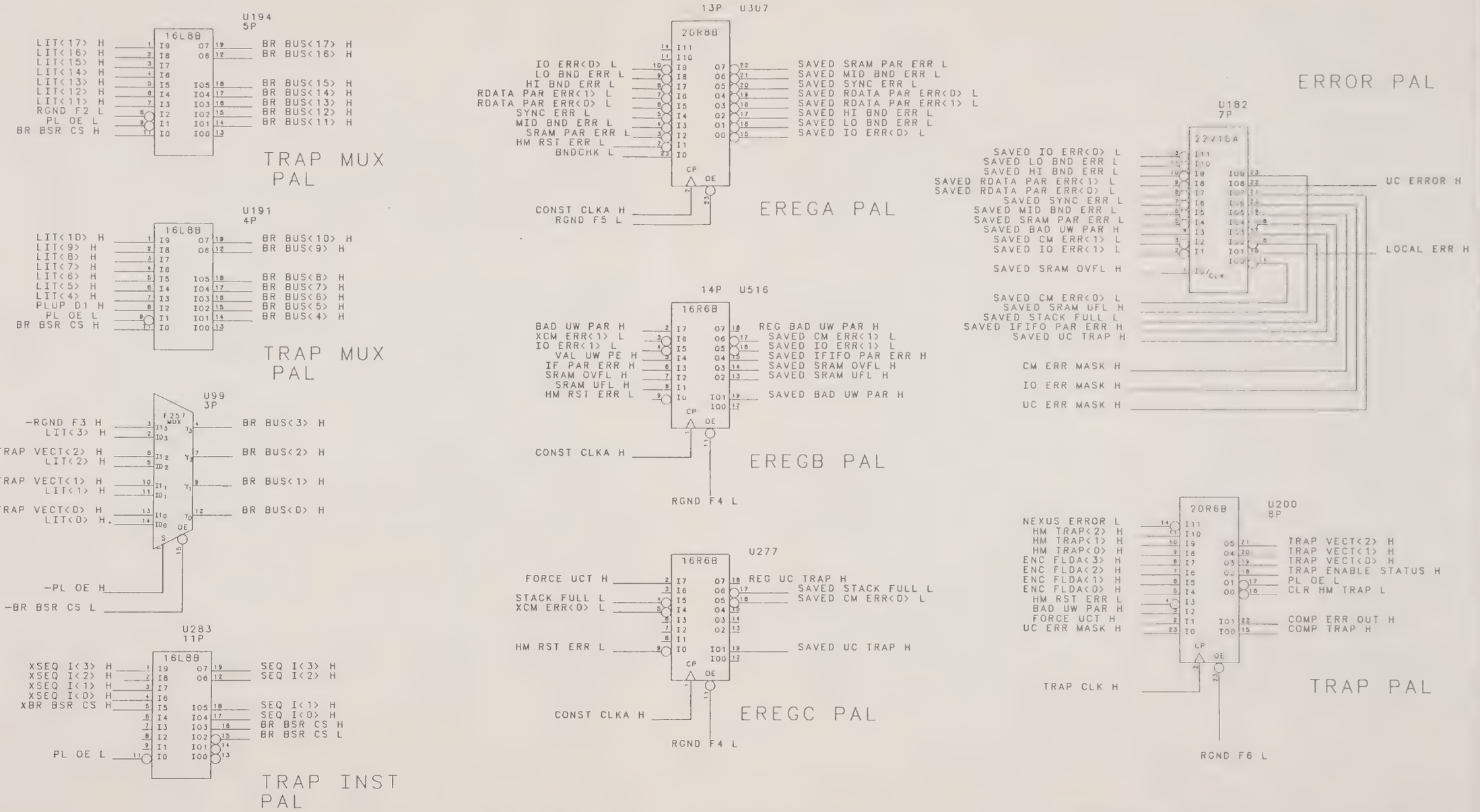
TITLE: MICROSEQUENCER, DISPATCH REGISTER AND CONDITION CODE MUX REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY:

PAGE: 21



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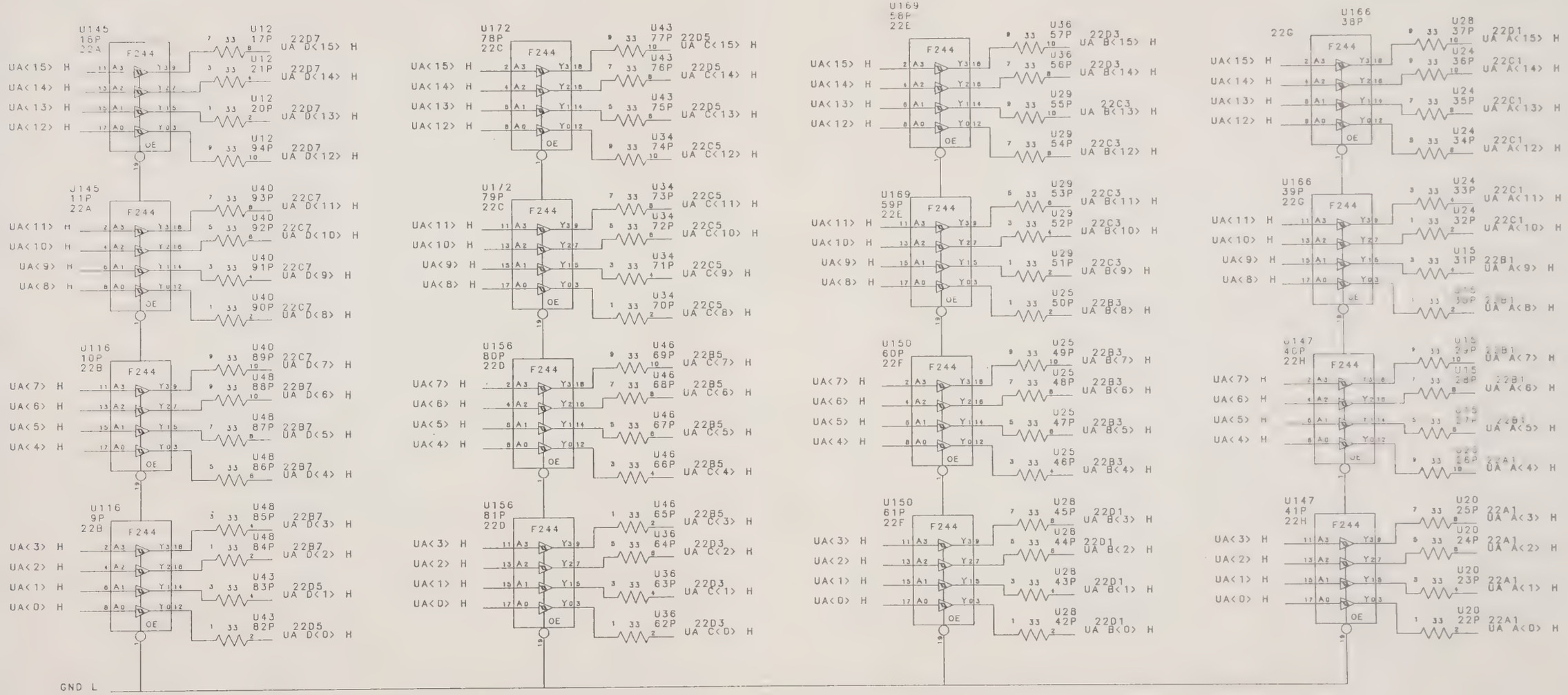
TITLE: TRAP LOGIC REV 4	DATE: 7/11/87
ENGINEER:	DRAWN BY: t.moser
	PAGE: 22



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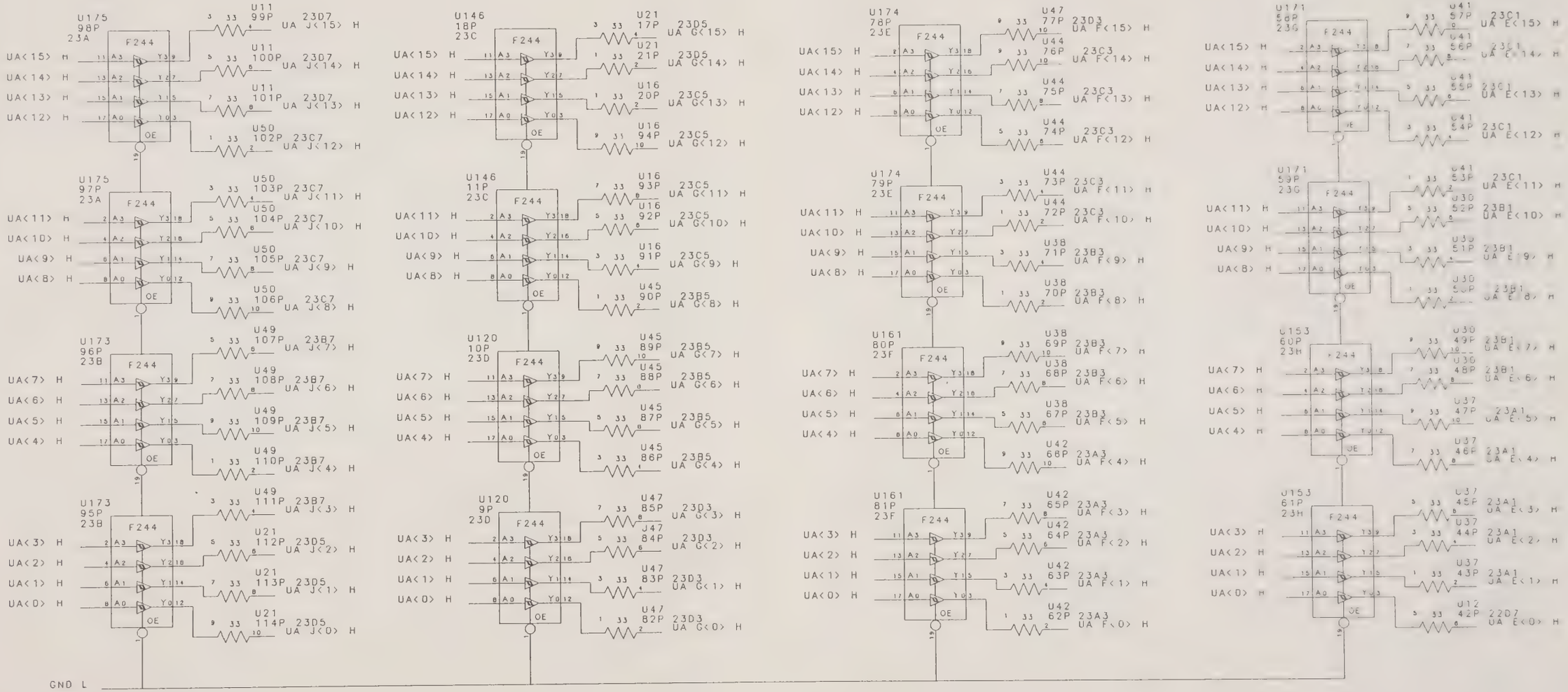
TITLE: CONTROL STORE ADDRESS BUFFERS (1 OF 2) REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser

PAGE: 23



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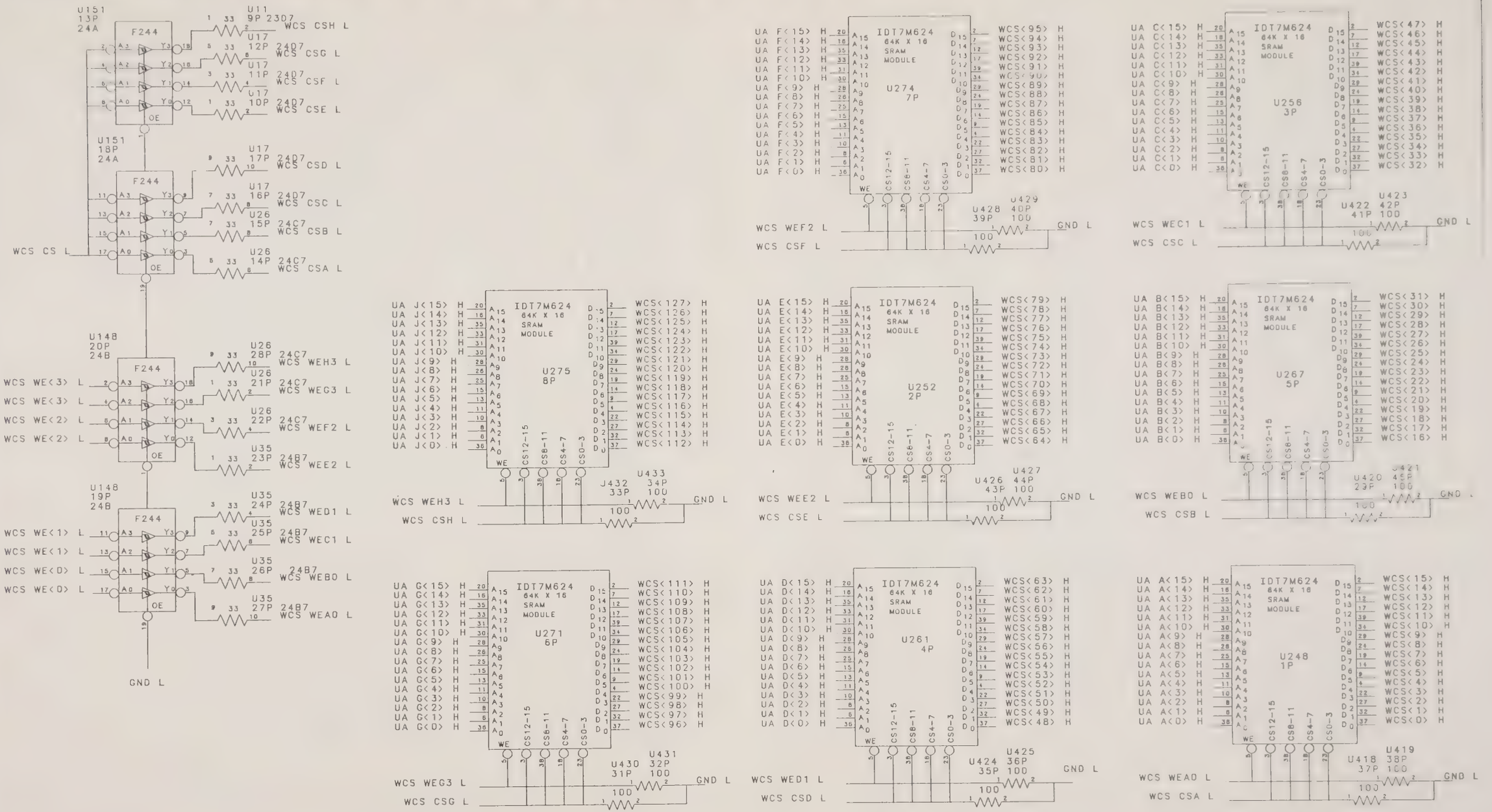
TITLE: CONTROL STORE ADDRESS BUFFERS (2 OF 2) REV 4

ENGINEER:

DRAWN BY:

DATE: 7/11/87



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TITLE:		DATE:
CONTROL STORE REV 4		7/11/87
ENGINEER:	DRAWN BY:	PAGE: 25

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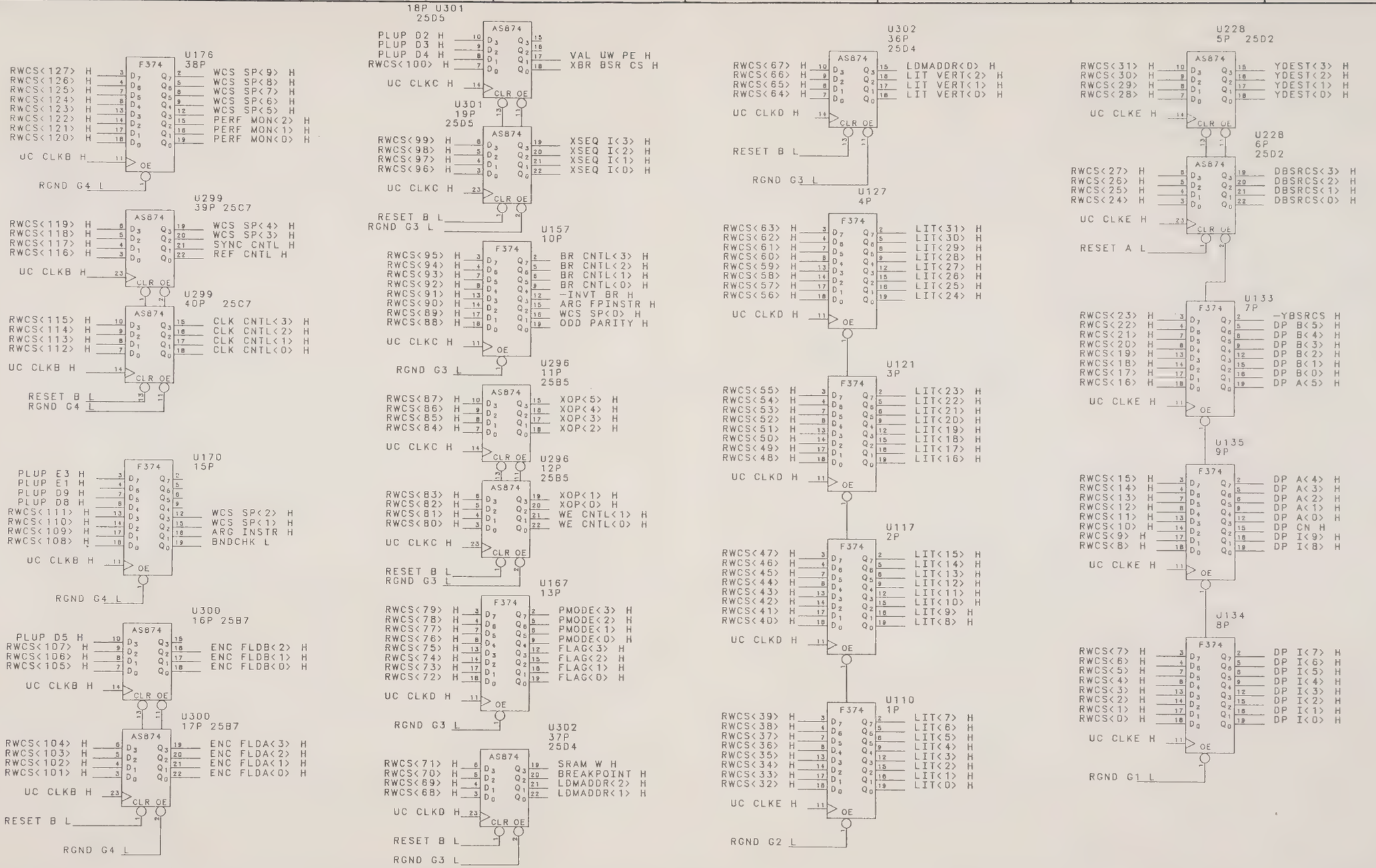
TITLE: BETA MICRO CONTROL STORE TERMINATORS		DATE: 7/11/87
ENGINEER:	DRAWN BY: t.moser	PAGE: 26



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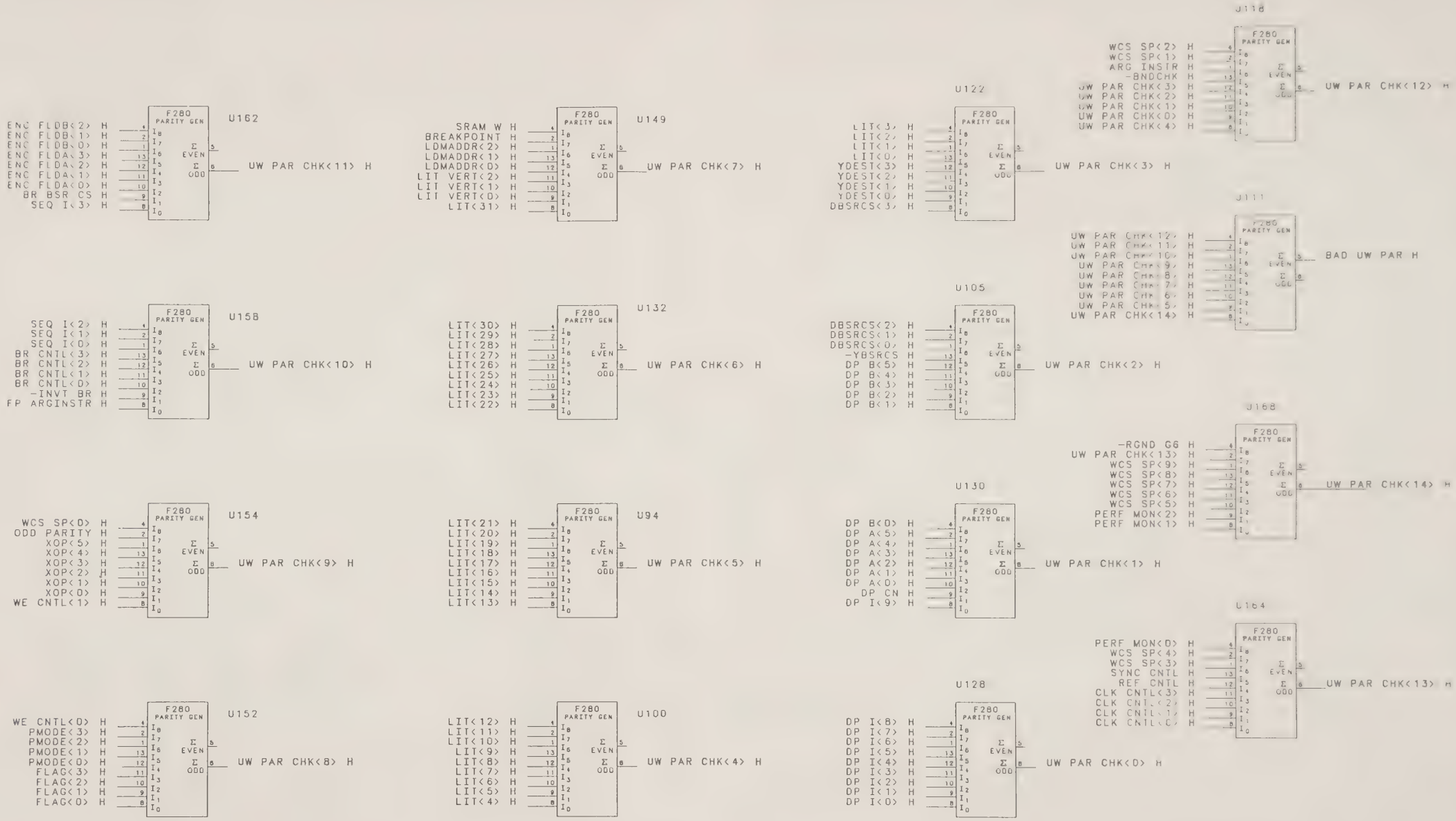
TITLE: PIPELINE REGISTER REV 4	DATE: 7/11/87
ENGINEER:	DRAWN BY:
	PAGE: 27



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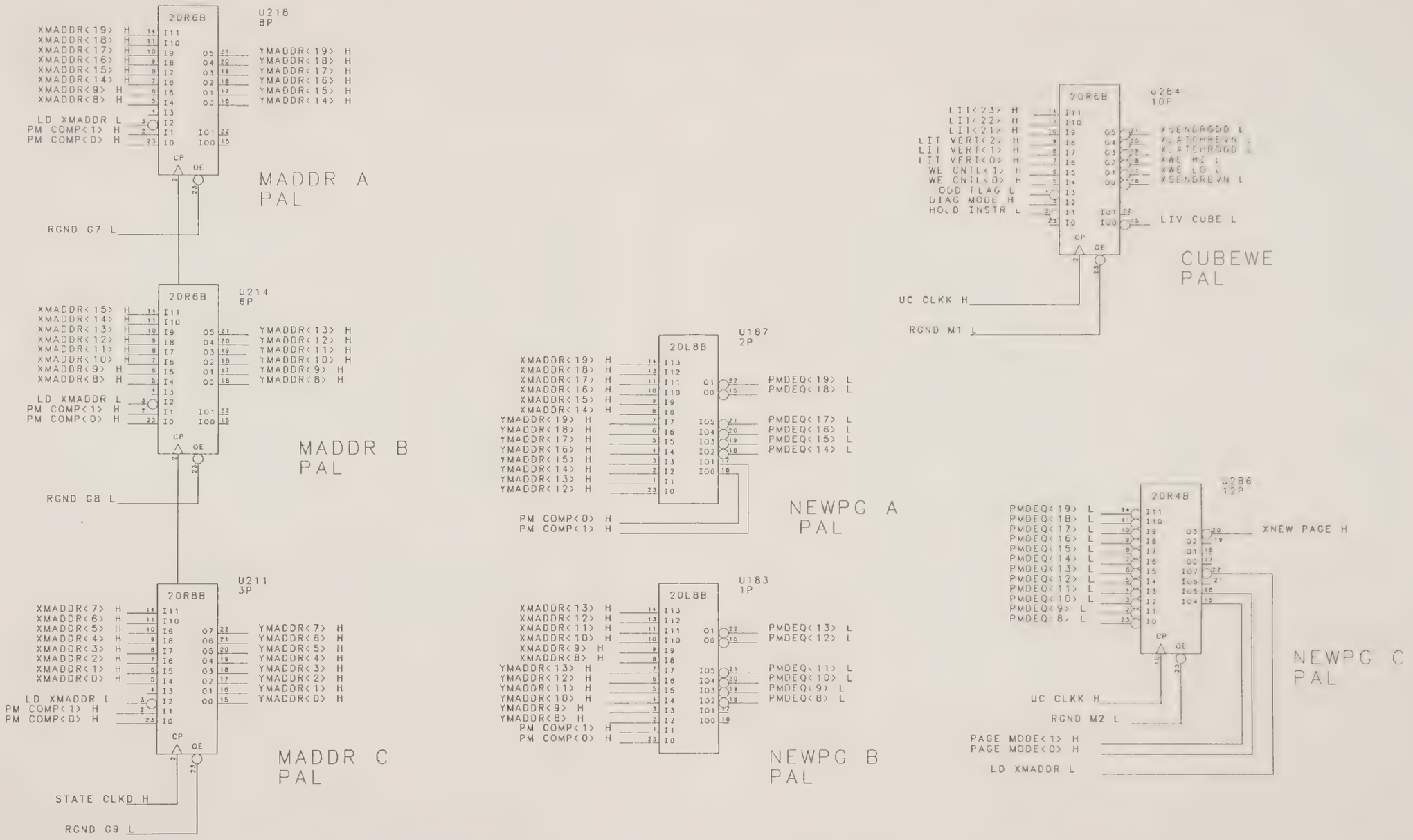
TITLE: CONTROL STORE PARITY CHECK
REV 4

ENGINEER:

DRAWN BY: t.moser

DATE: 7/11/87

PAGE: 28



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TITLE: MADDR REGISTERS, NEW PAGE LOGIC & CUBE CONTROL REV 4

DATE: 7/11/87

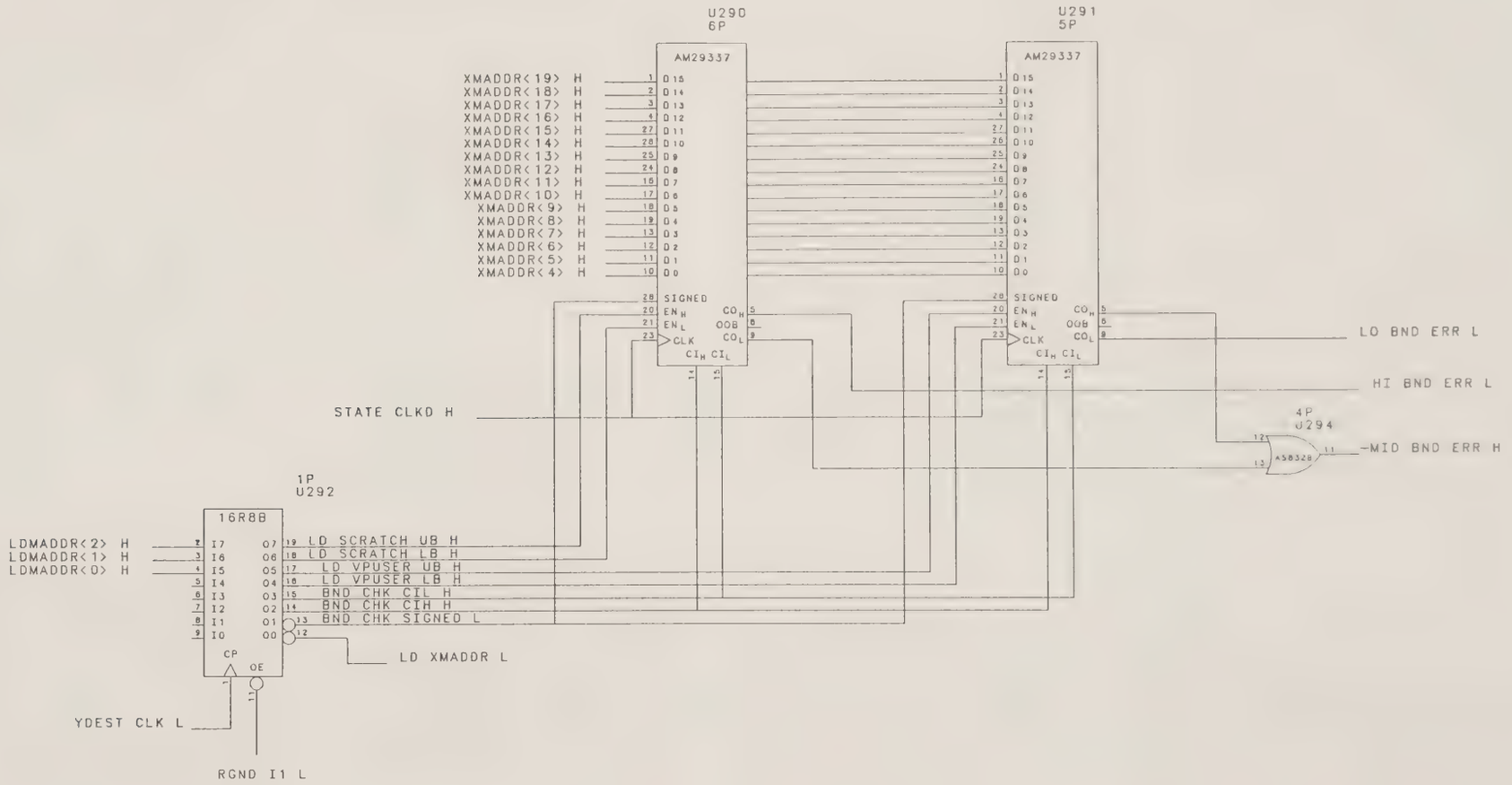
ENGINEER:

DRAWN BY:

PAGE: 29

SCRATCH MEMORY BOUNDS COMPARATOR

VP/USR BOUNDS COMPARATOR



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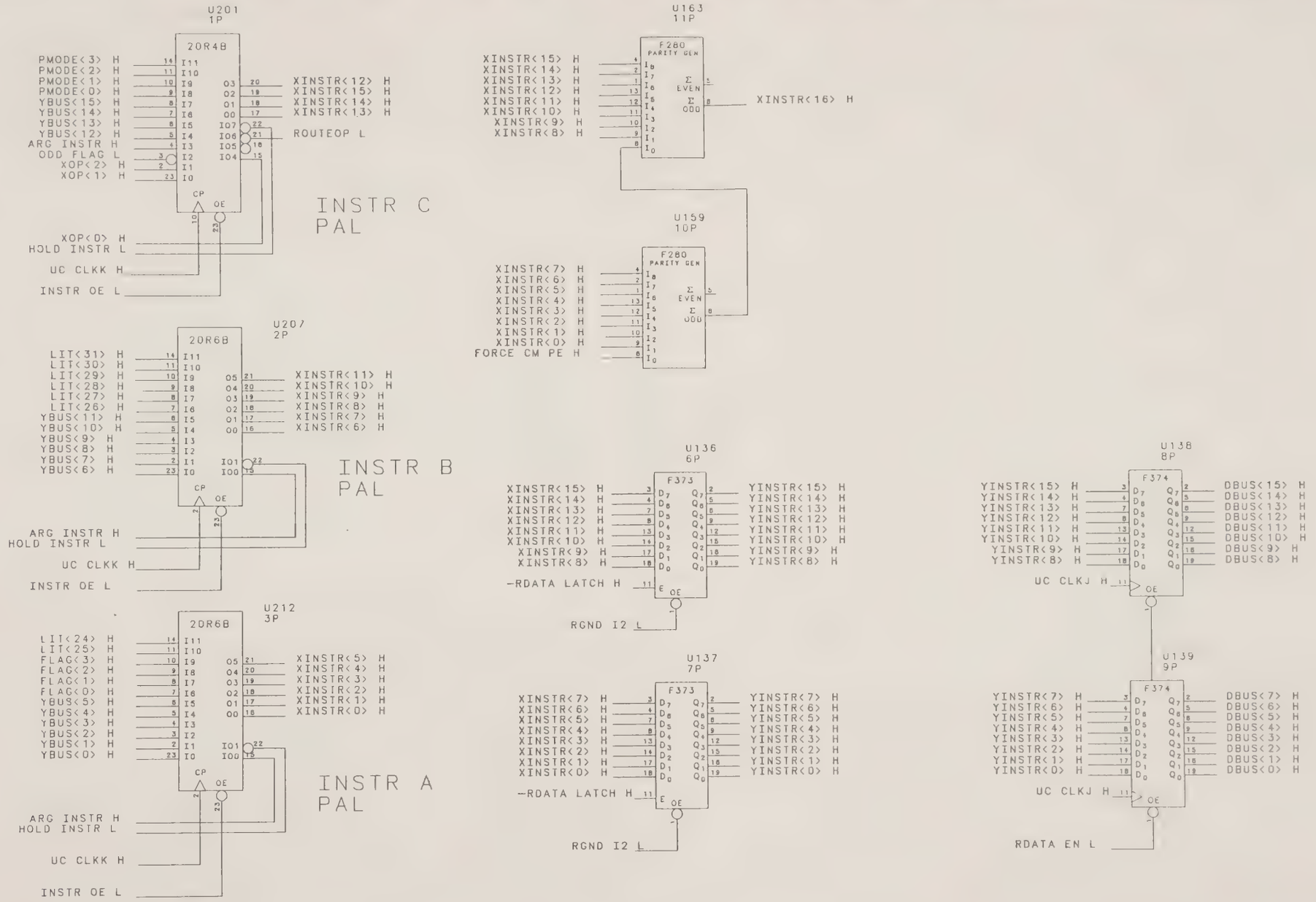
TITLE: VP/USER & SCRATCH MEMORY UPPER & LOWER BOUNDS COMPARATORS REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY:

PAGE: 30



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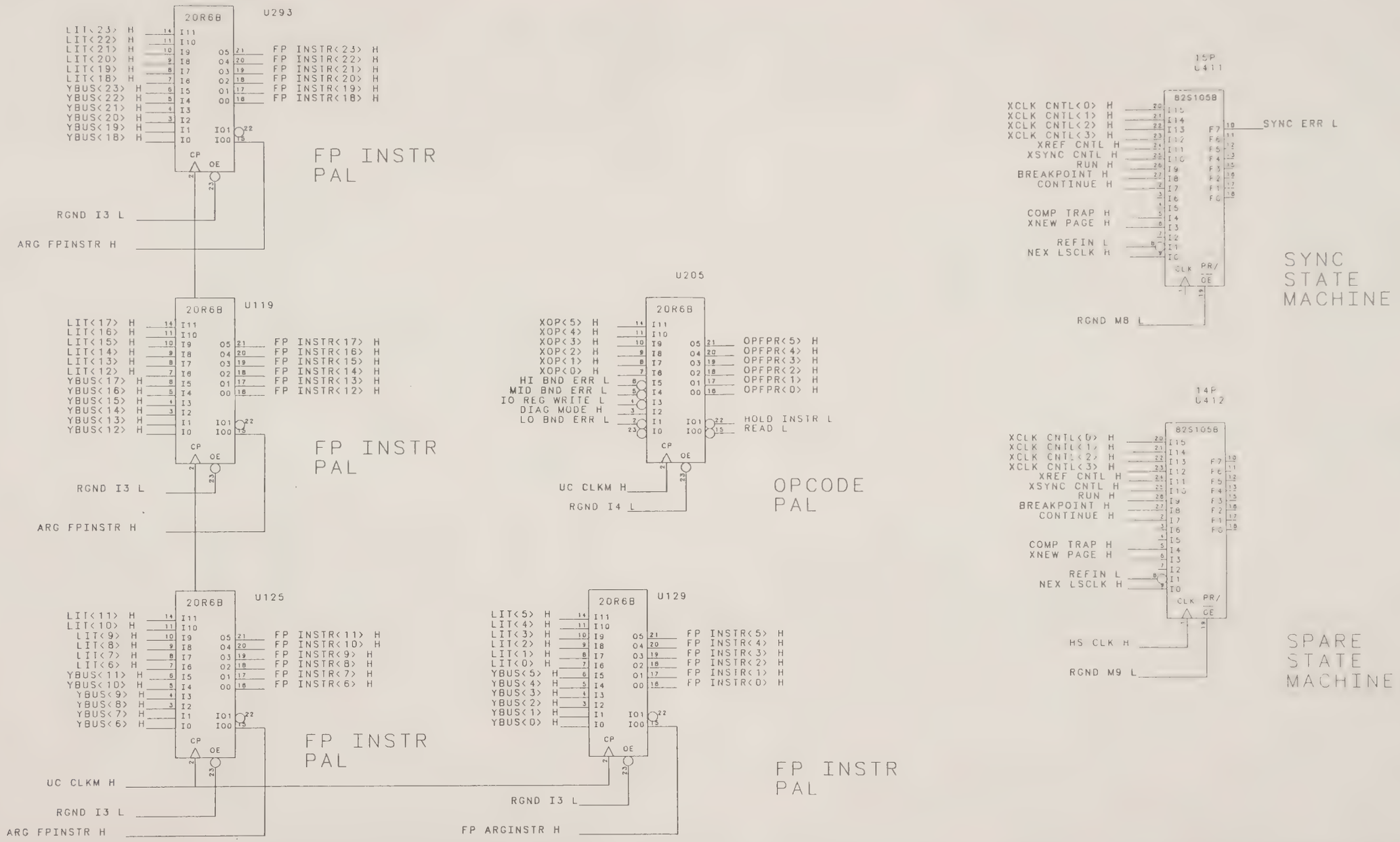
TITLE: INSTR GENERATION AND PARITY AND RDATA REGISTER REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY: t.moser



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TITLE: FLOATING POINT REGISTER/MUX AND SYNC STATE MACHINE REV 4

DATE: 7/11/87

ENGINEER:

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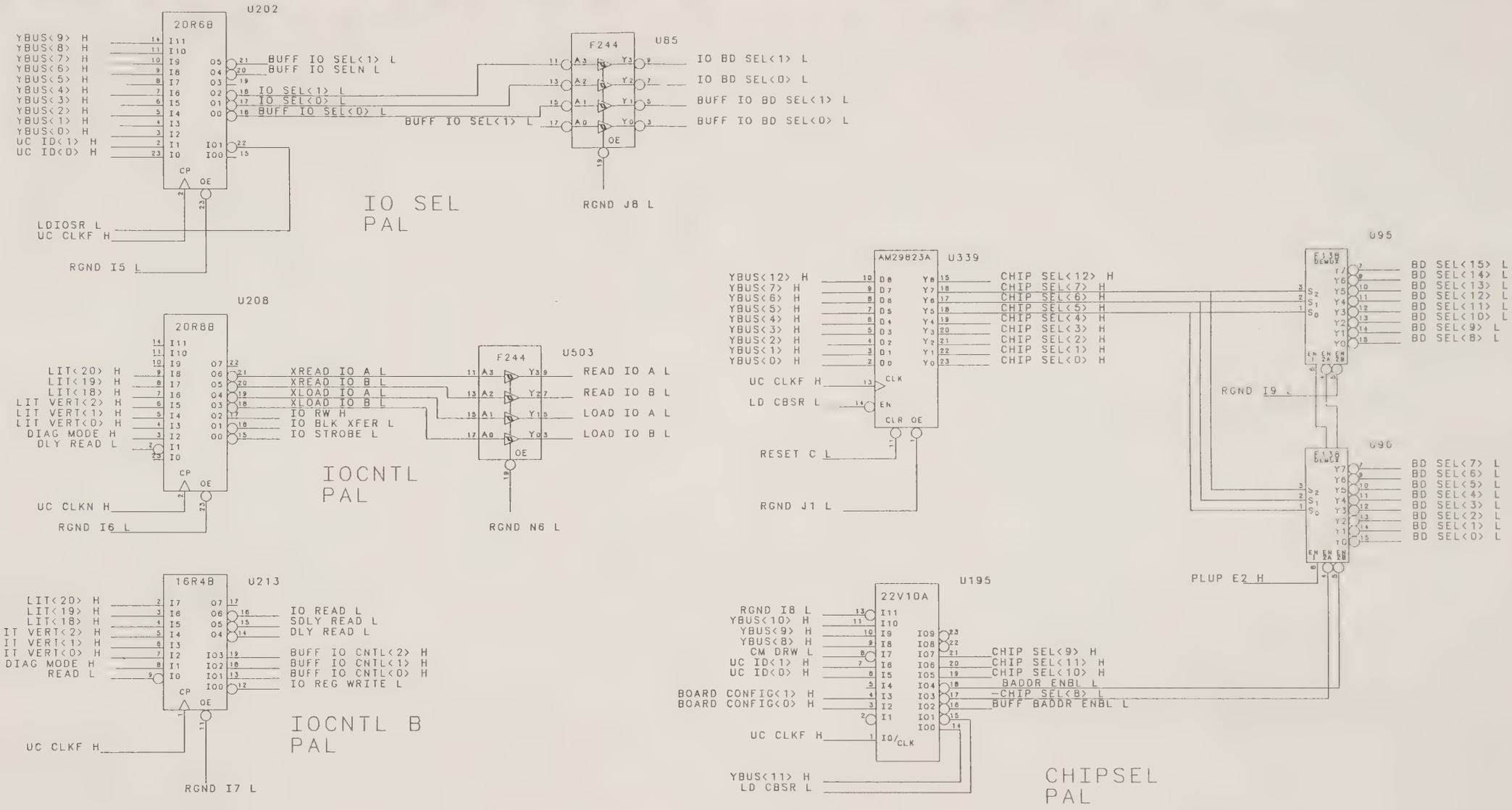

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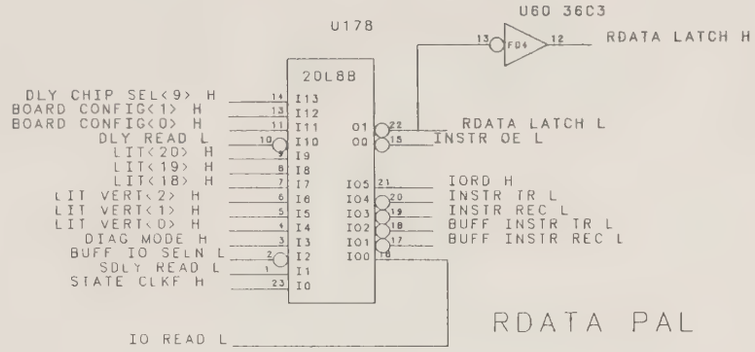
TITLE: IO CONTROL AND BOARD SELECT REV 4

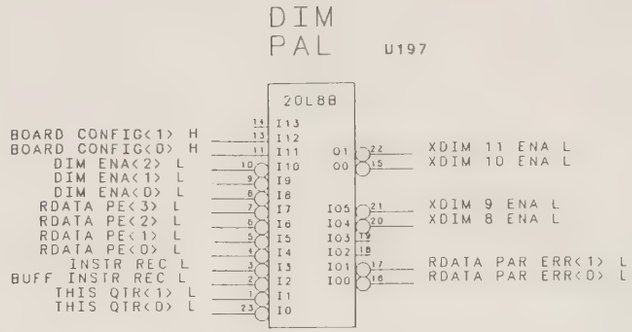
DATE: 7/11/87

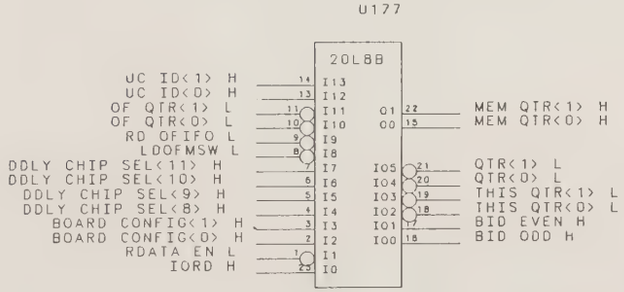
ENGINEER: JIM LALONE

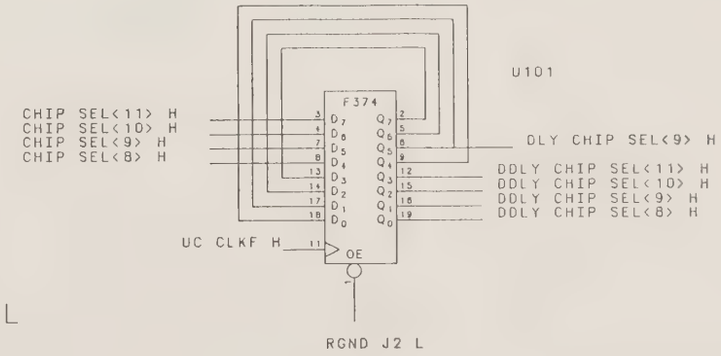
DRAWN BY:

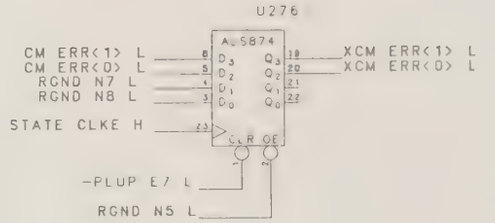
PAGE: 33

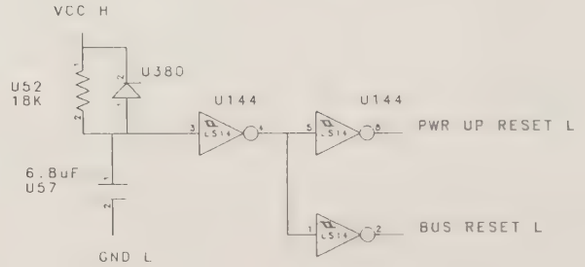












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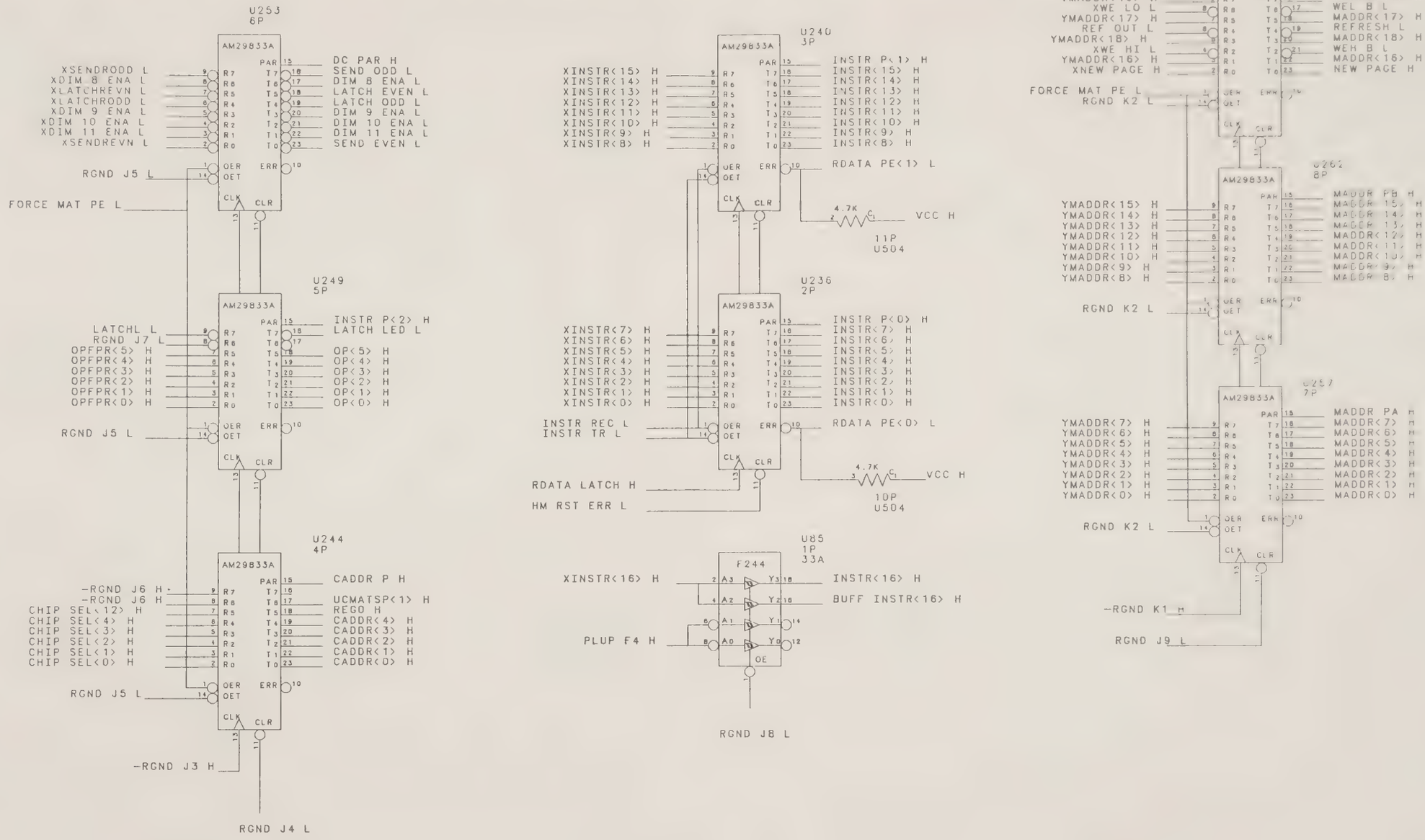
TITLE:		DATE:
RDATA CONTROL /ERROR LATCH REV 4		7/11/87
ENGINEER: JIM LALONE	DRAWN BY:	PAGE: 34



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TITLE: UC MATRIX TRANSIEVERS REV 4

DATE: 7/11/87

ENGINEER:

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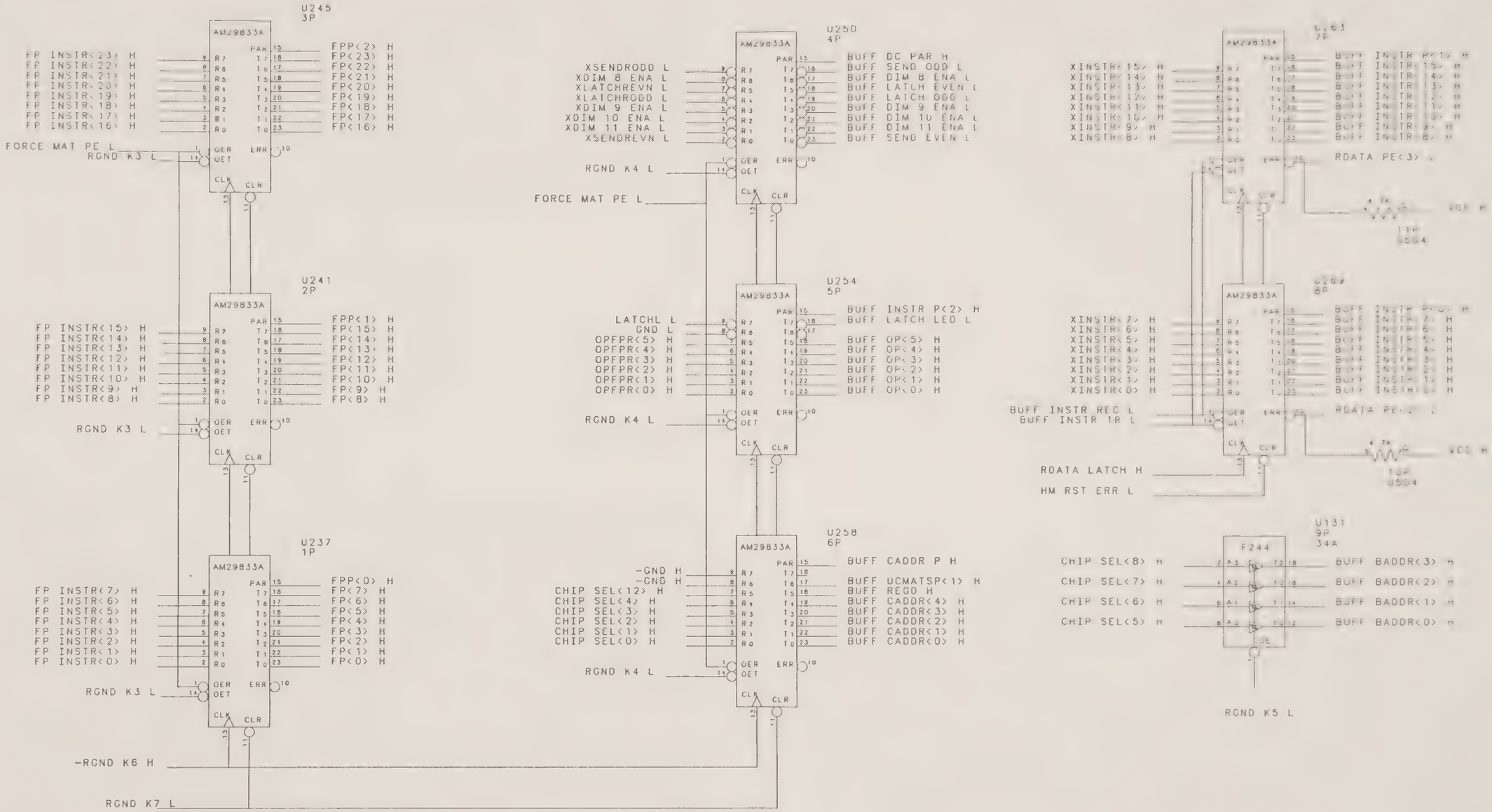

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TITLE: UC MATRIX TRANSIEVERS REV 4

DATE: 7/11/87

ENGINEER:

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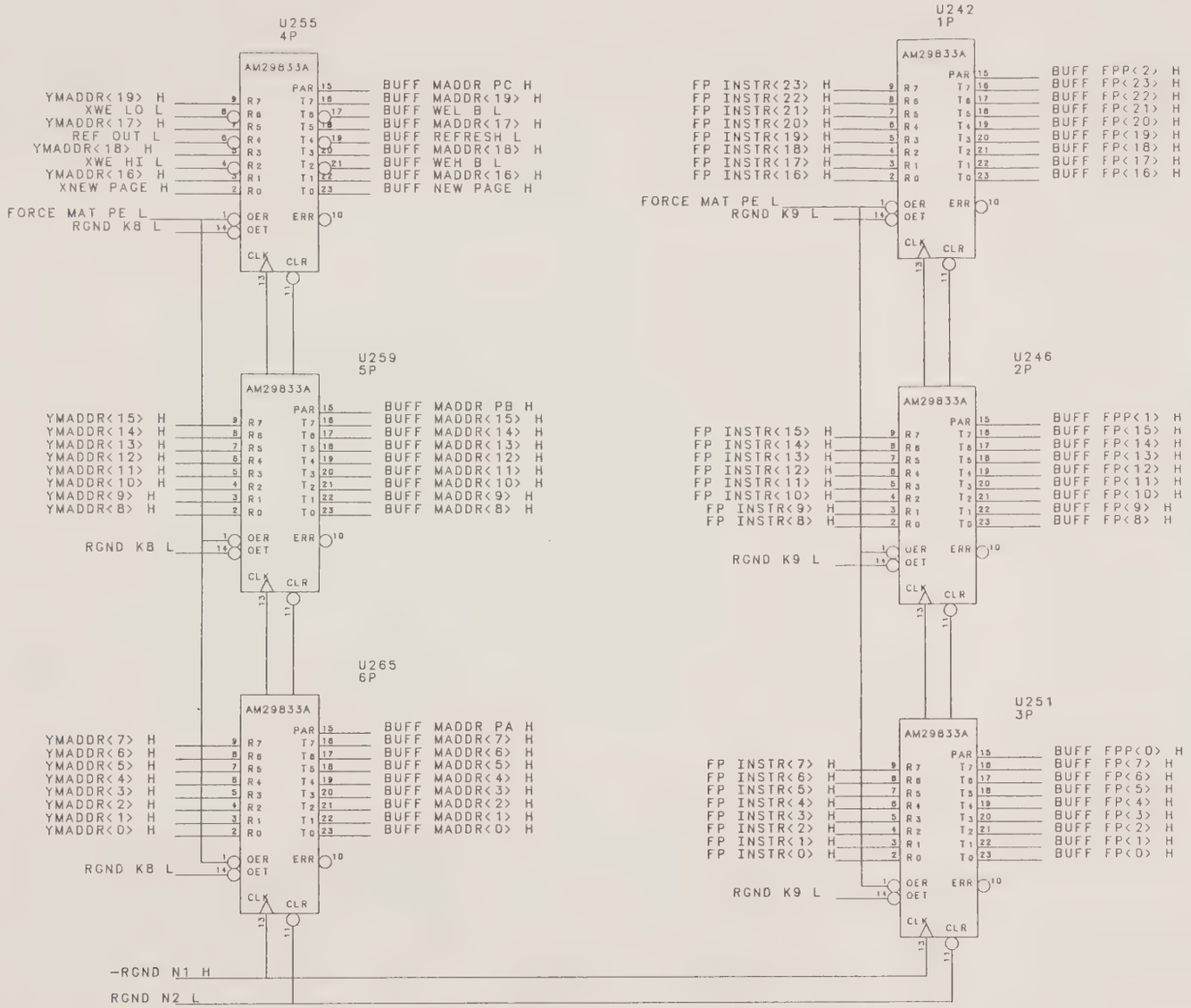
PAGE: 36



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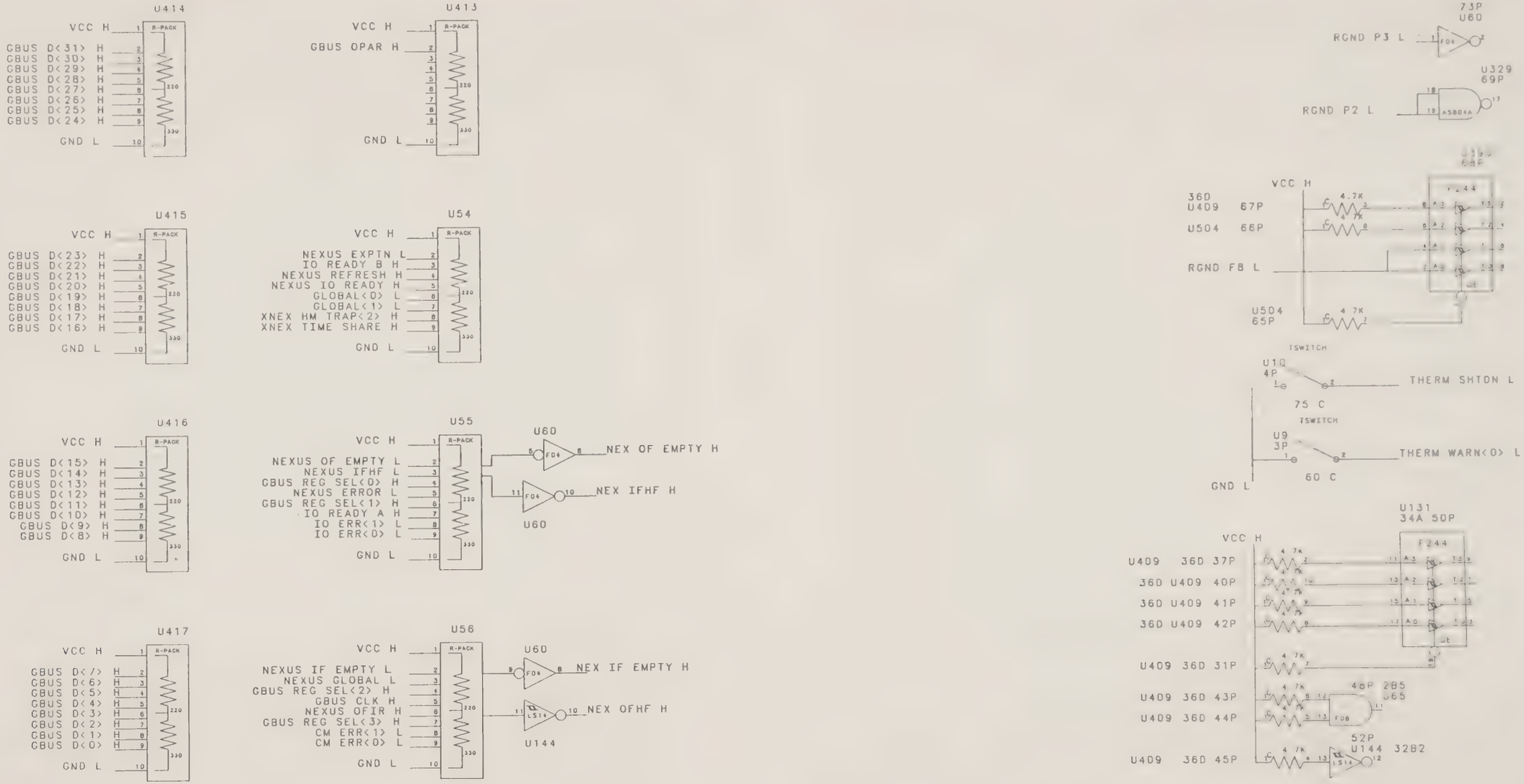
TITLE: UC BUFFER TRANSIEVERS		DATE: 7/11/87
ENGINEER:	DRAWN BY: t.moser	PAGE: 37



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TITLE: GBUS TERMINATORS & THERMAL SWITCHES AND SPARES REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY:

PAGE: 38

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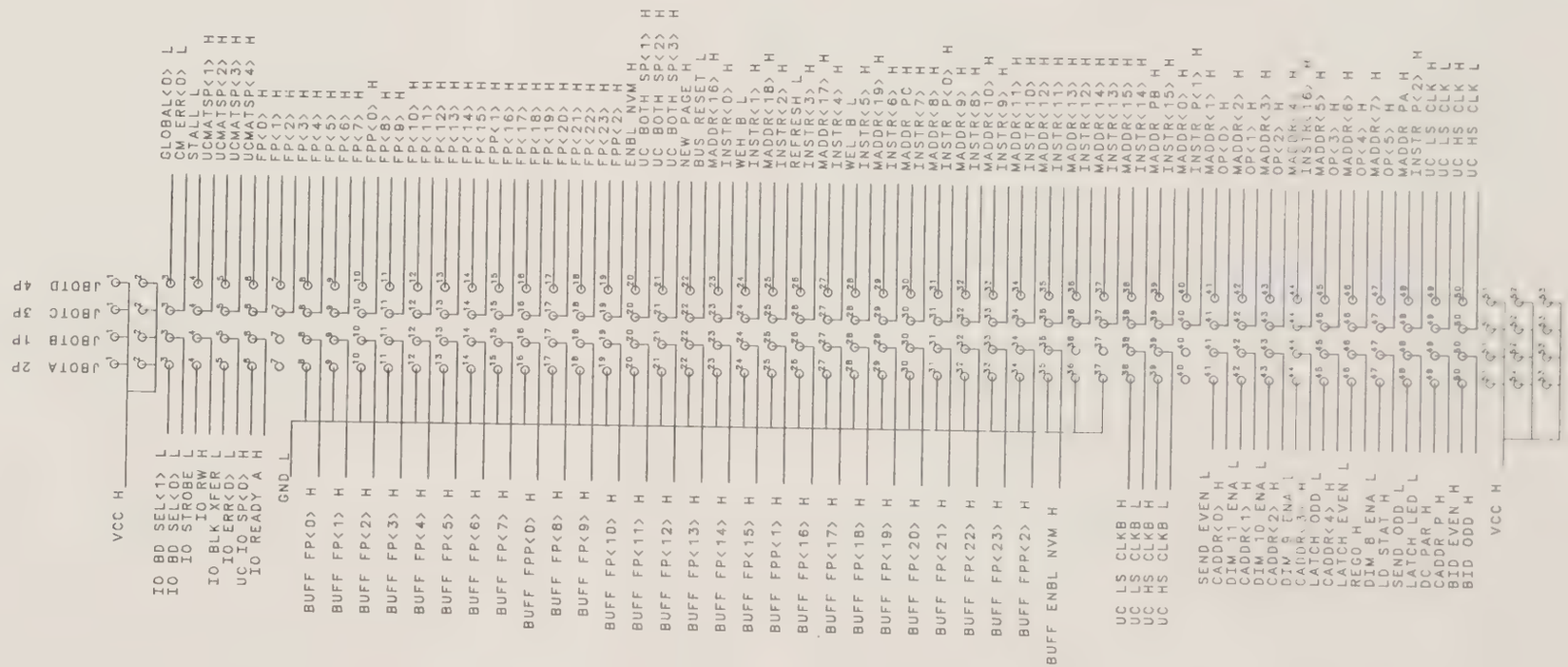
TITLE:	DATE:
PULL-UPS PULL-DOWNS REV 4	7/11/87
ENGINEER:	DRAWN BY: t.moser
	PAGE: 39



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TITLE: BACKPLANE CONNECTOR
SHEET 1 OF 3
JBOT
REV 4

DATE: 7/11/87

ENGINEER:

DRAWN BY:

PAGE: 40

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TITLE: BACKPLANE CONNECTOR SHEET 2 OF 3

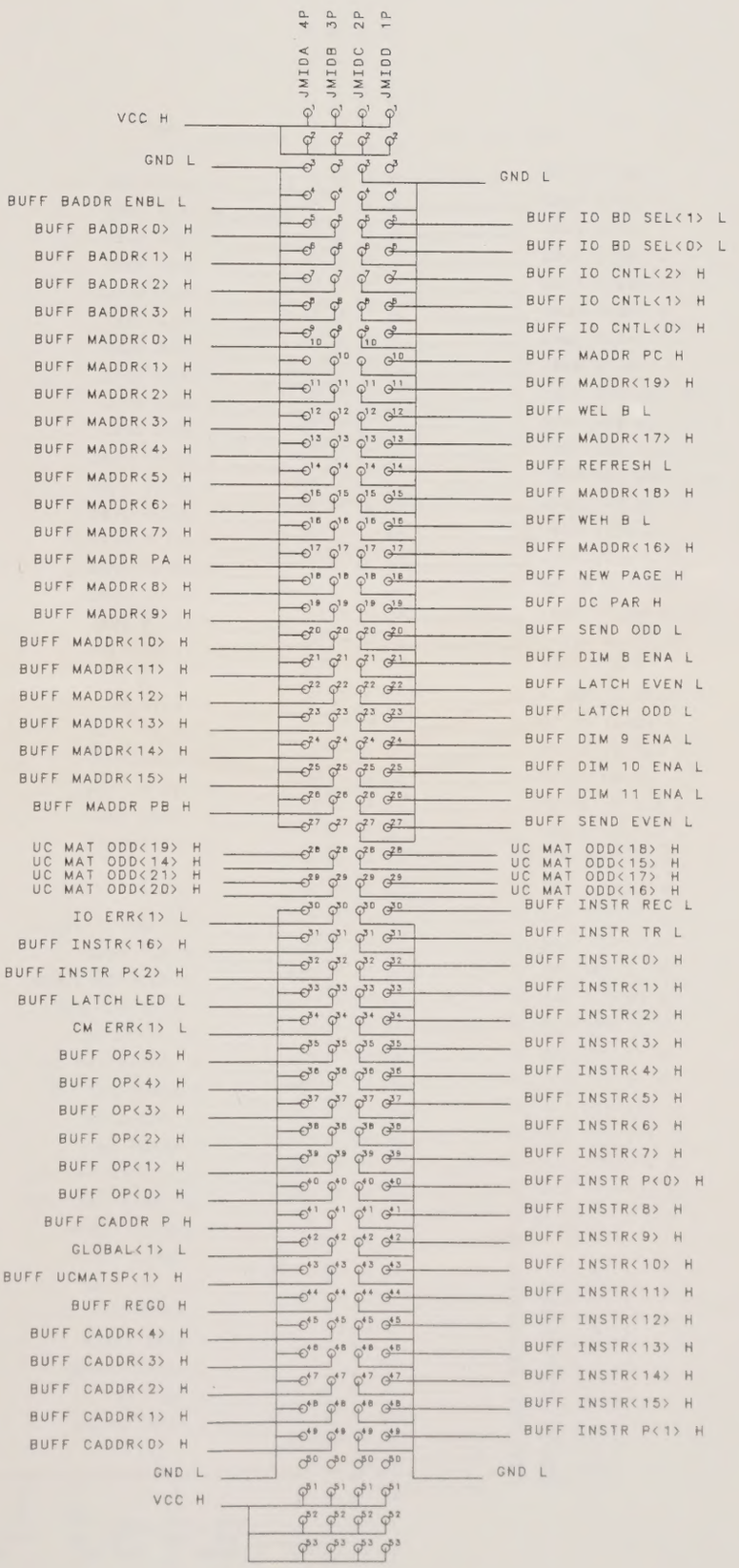
ENGINEER:

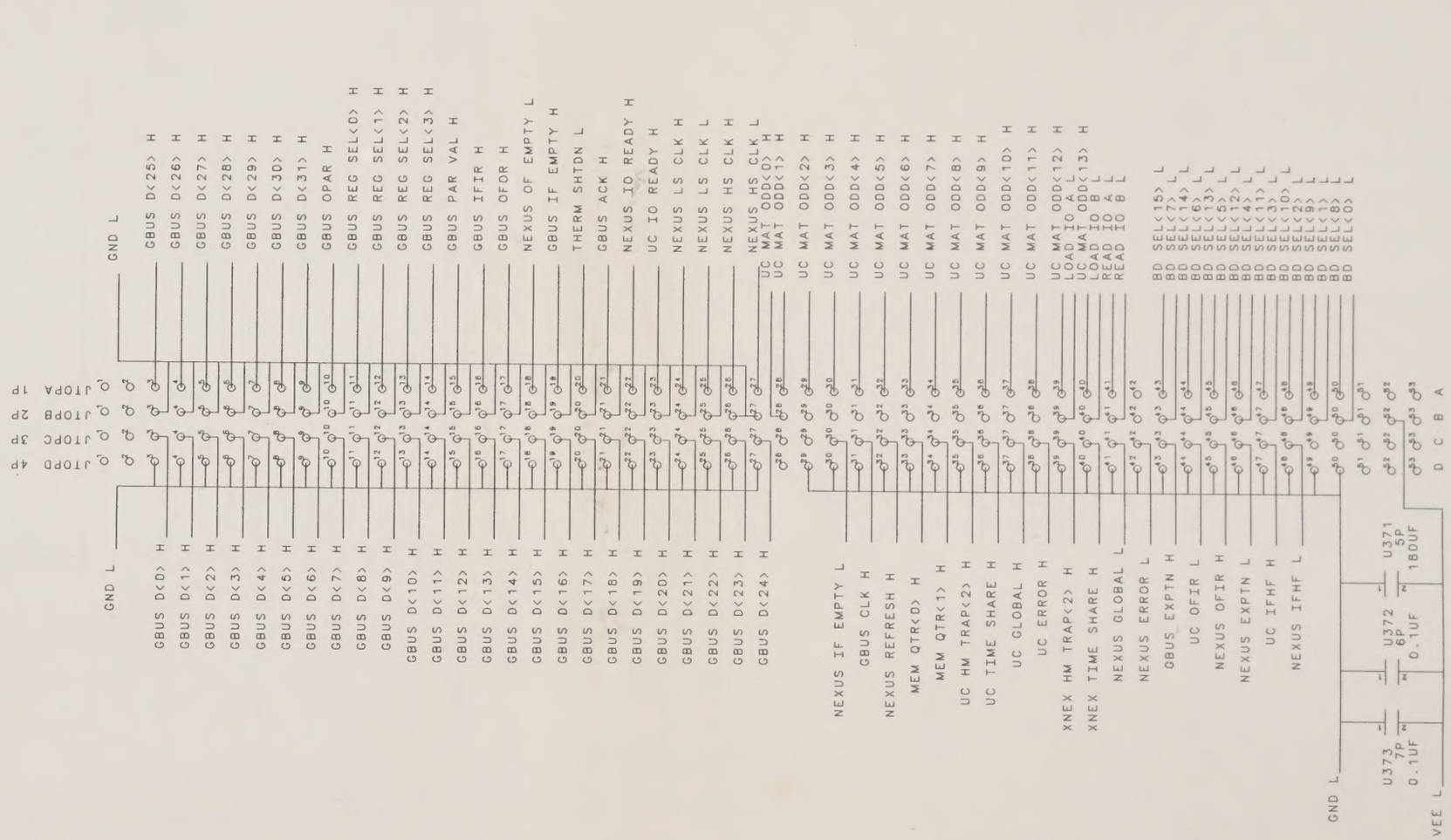
JMID REV 4

DRAWN BY:

DATE: 7/11/87

PAGE: 41





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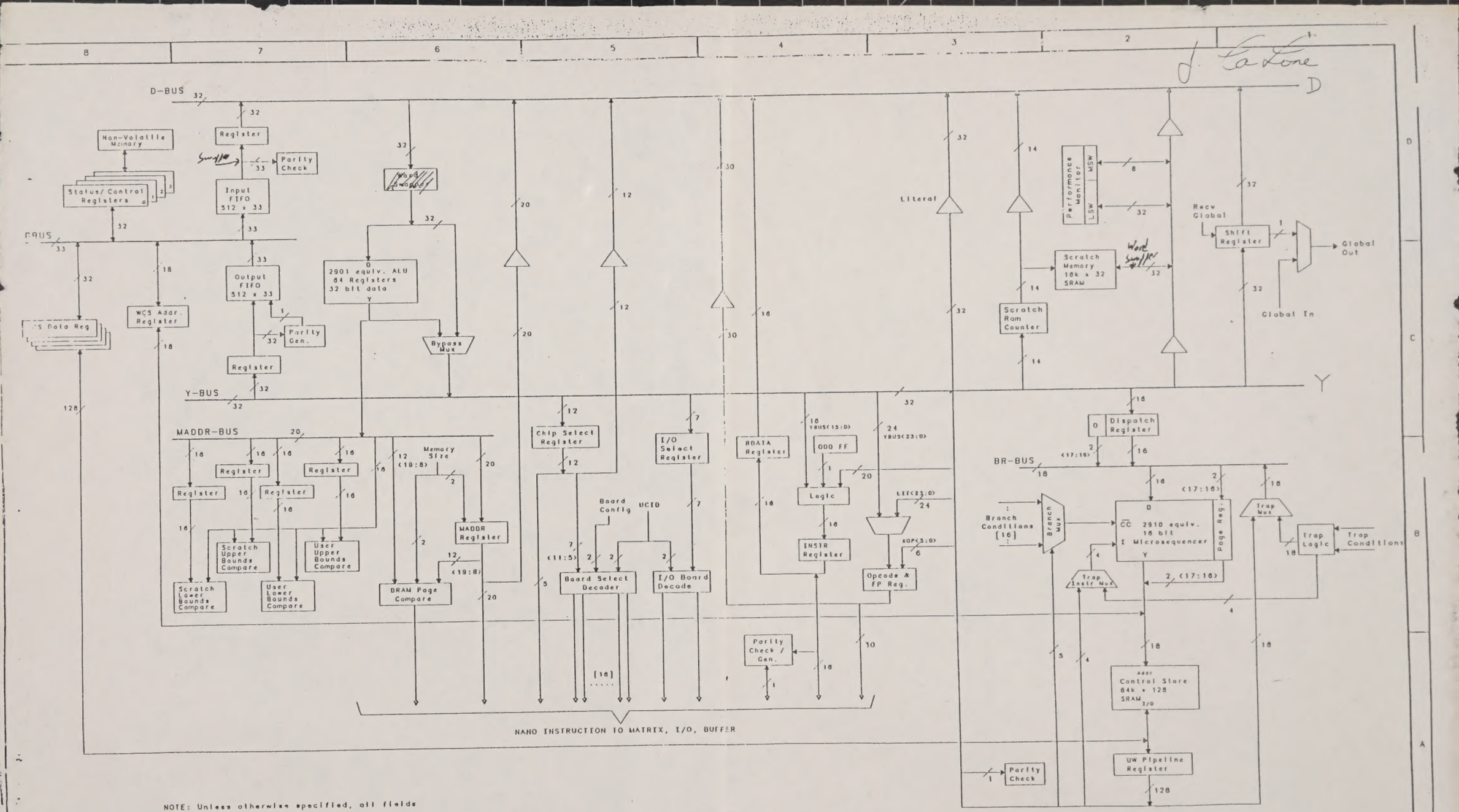
TITLE: BACKPLANE CONNECTOR SHEET 3 OF 3 — JTOP REV 4

ENGINEER:

DRAWN BY:

DATE: 7/11/87



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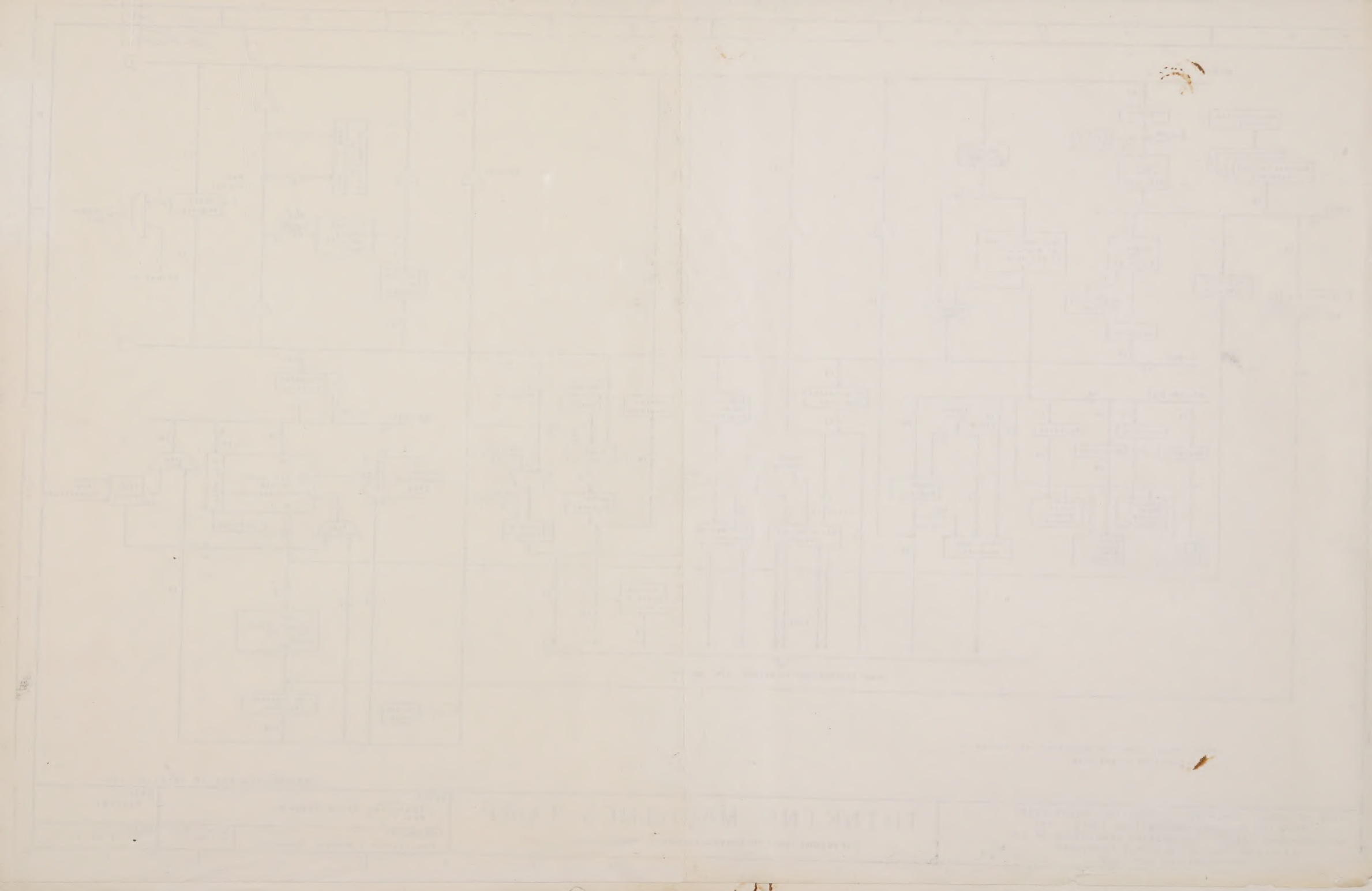
TITLE: Sequencer Block Diagram Rev 4

DATE: 8/25/87

ENGINEER: Jim Lotona / Mahesh Ganmukhi

DRAWN BY: t.m.

PAGE: 1 of 1